

FIG. 1

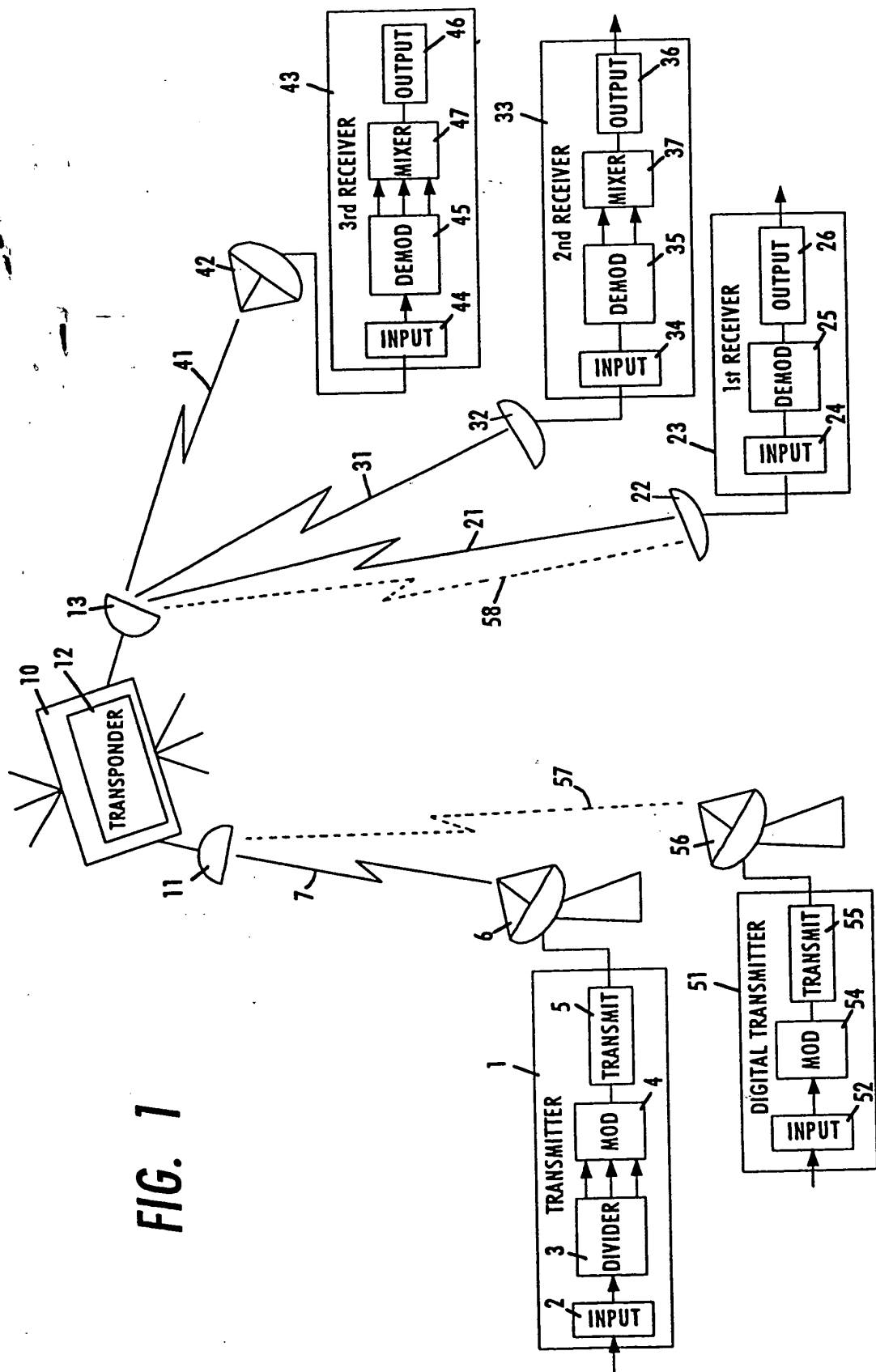
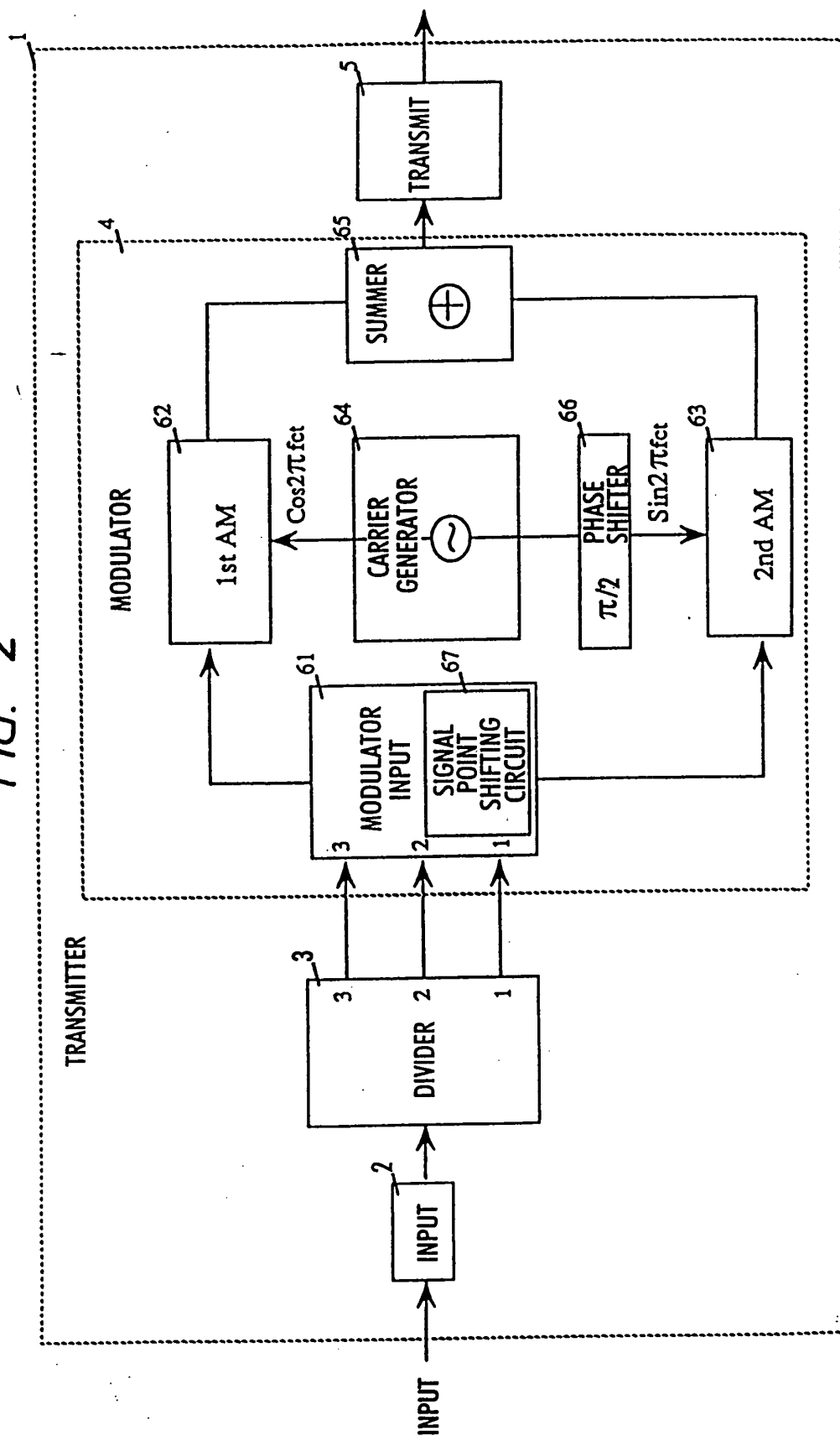
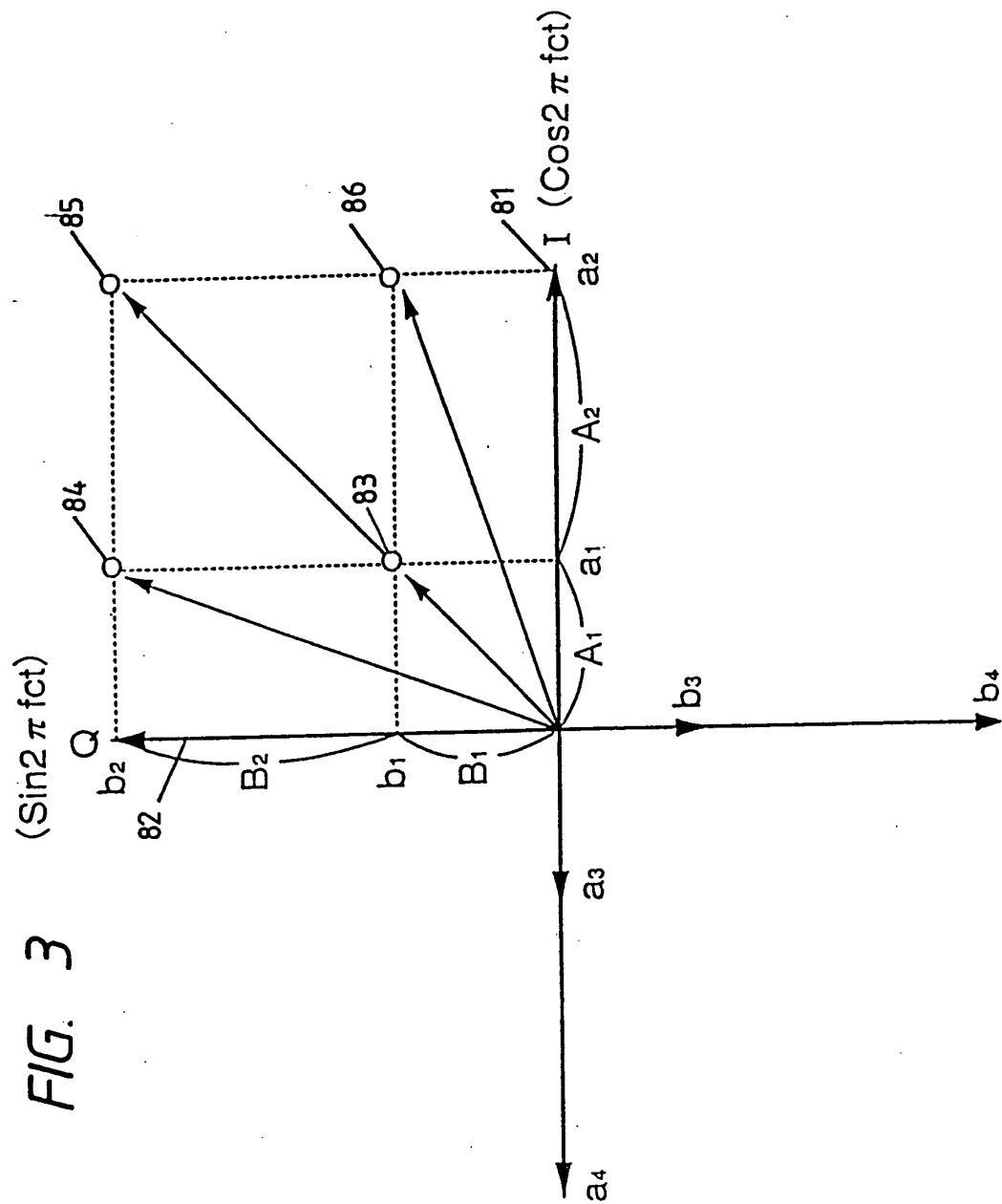
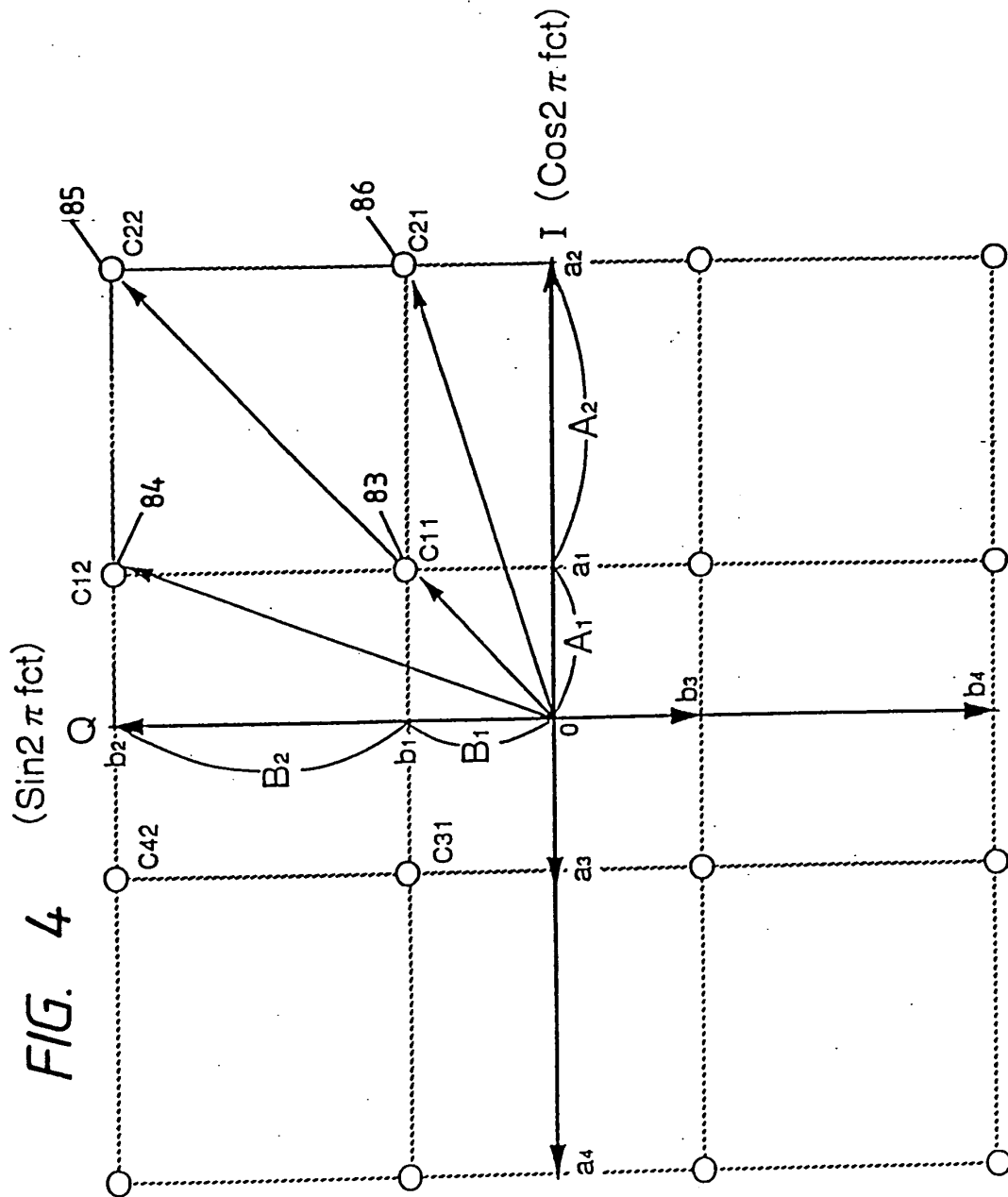


FIG. 2







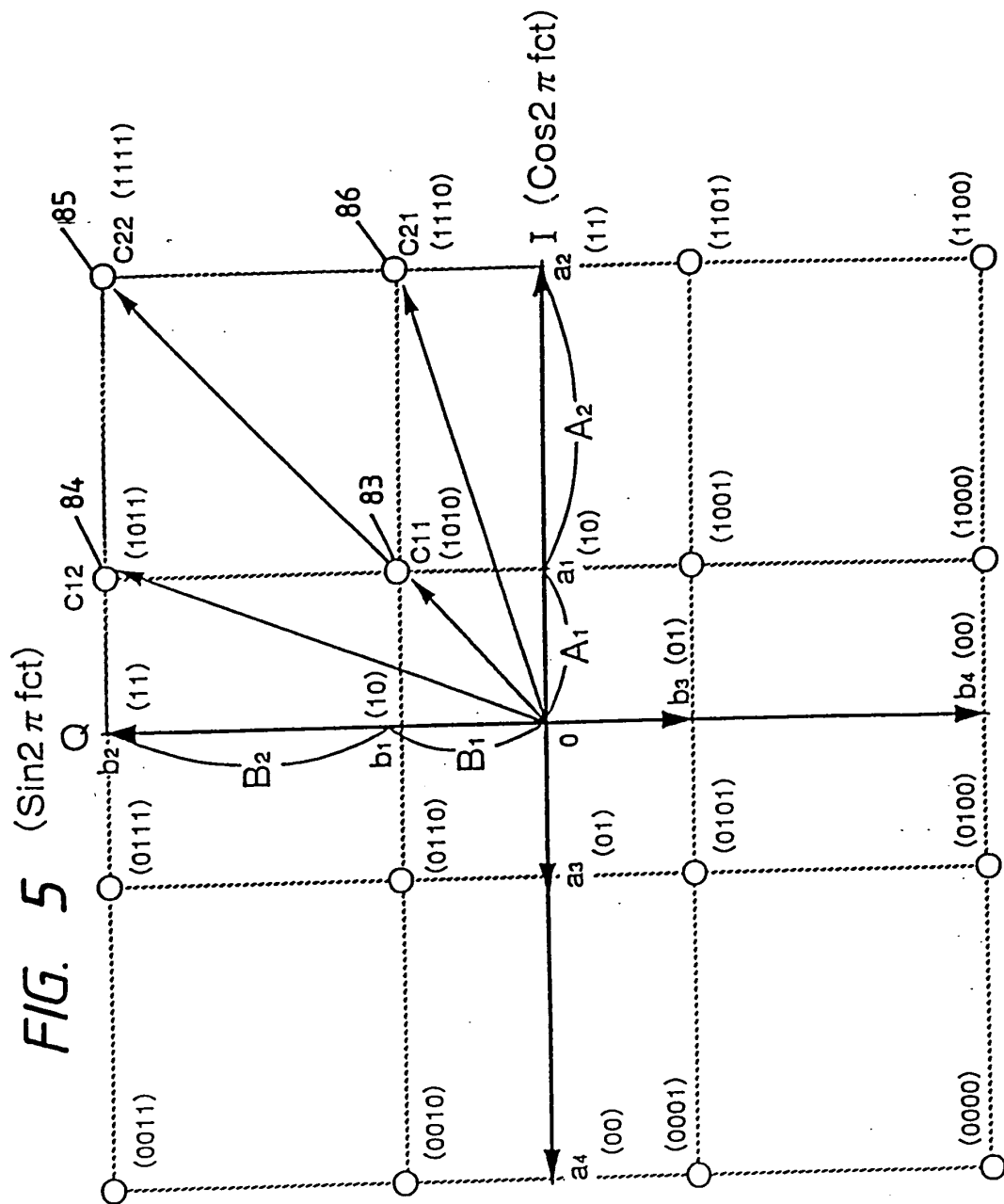


FIG. 6

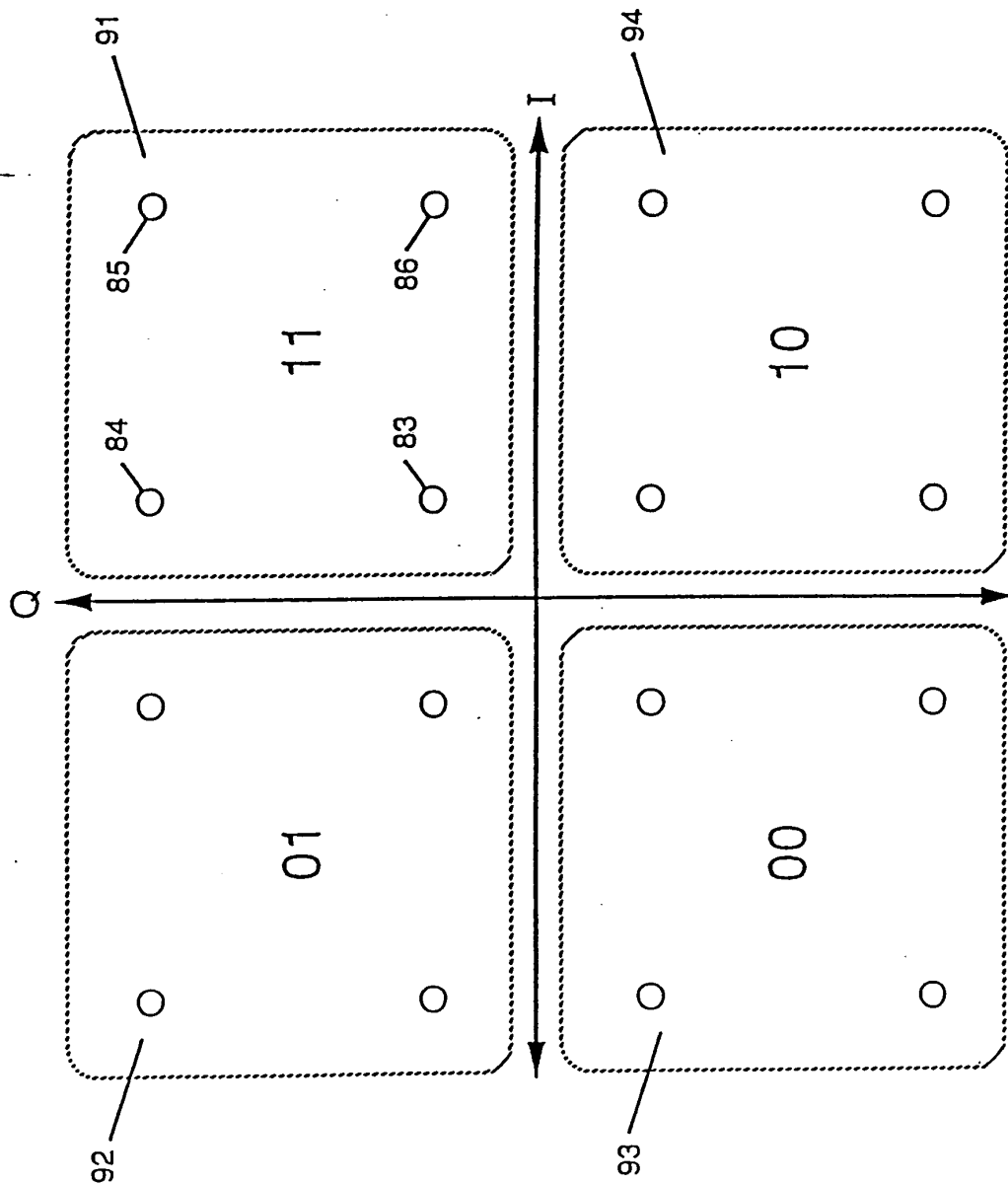


FIG. 7

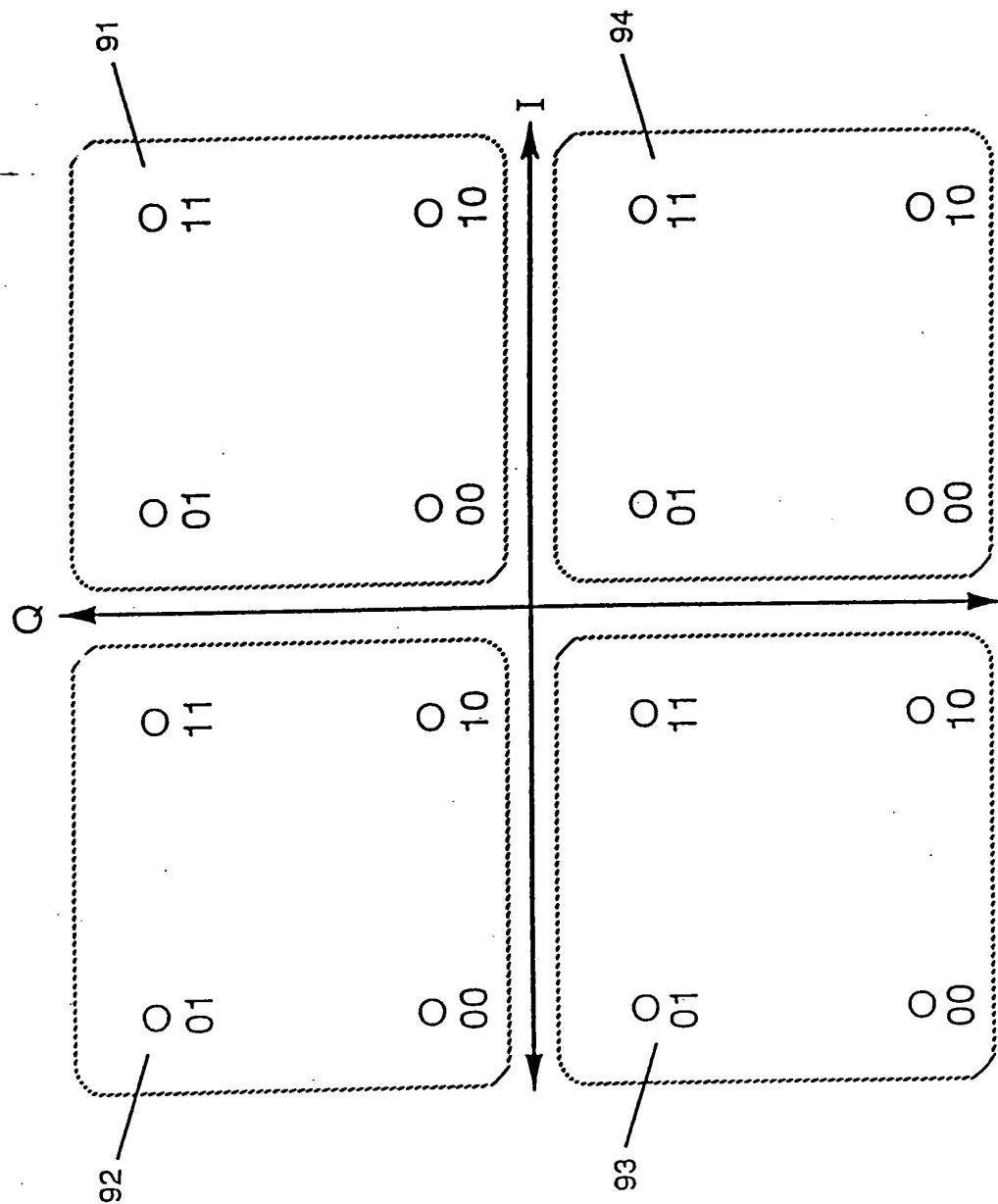


FIG. 8

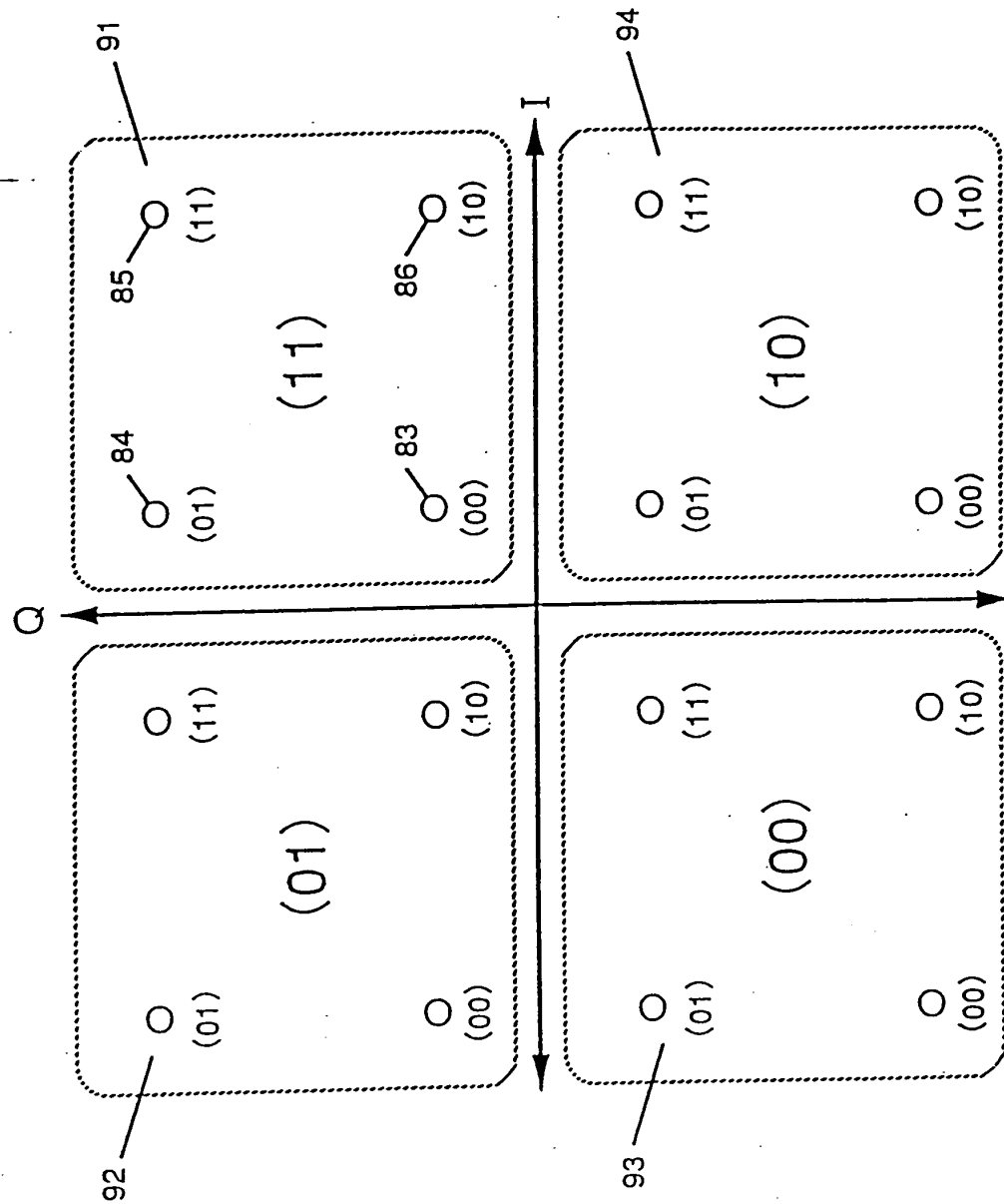


FIG. 9

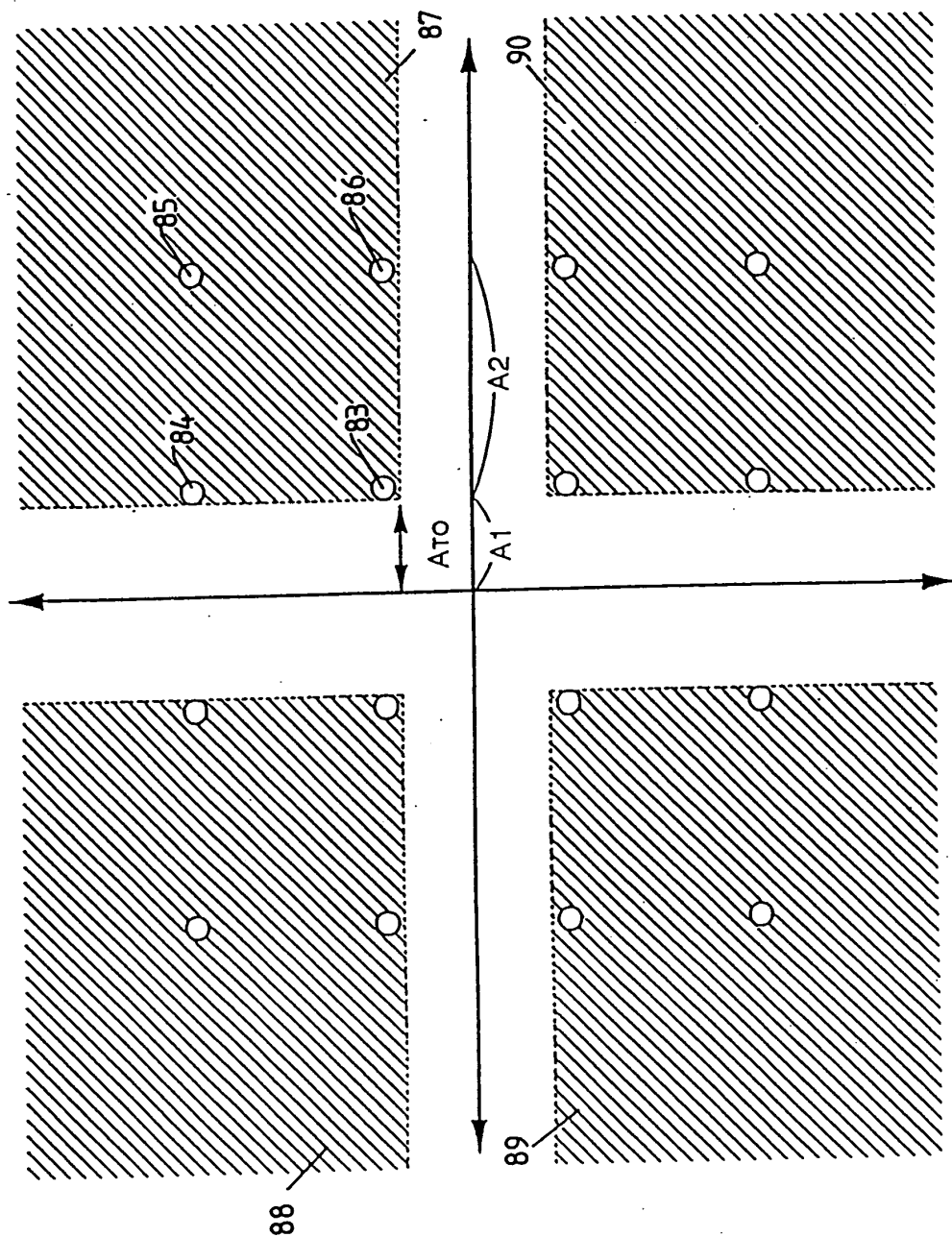


FIG. 10

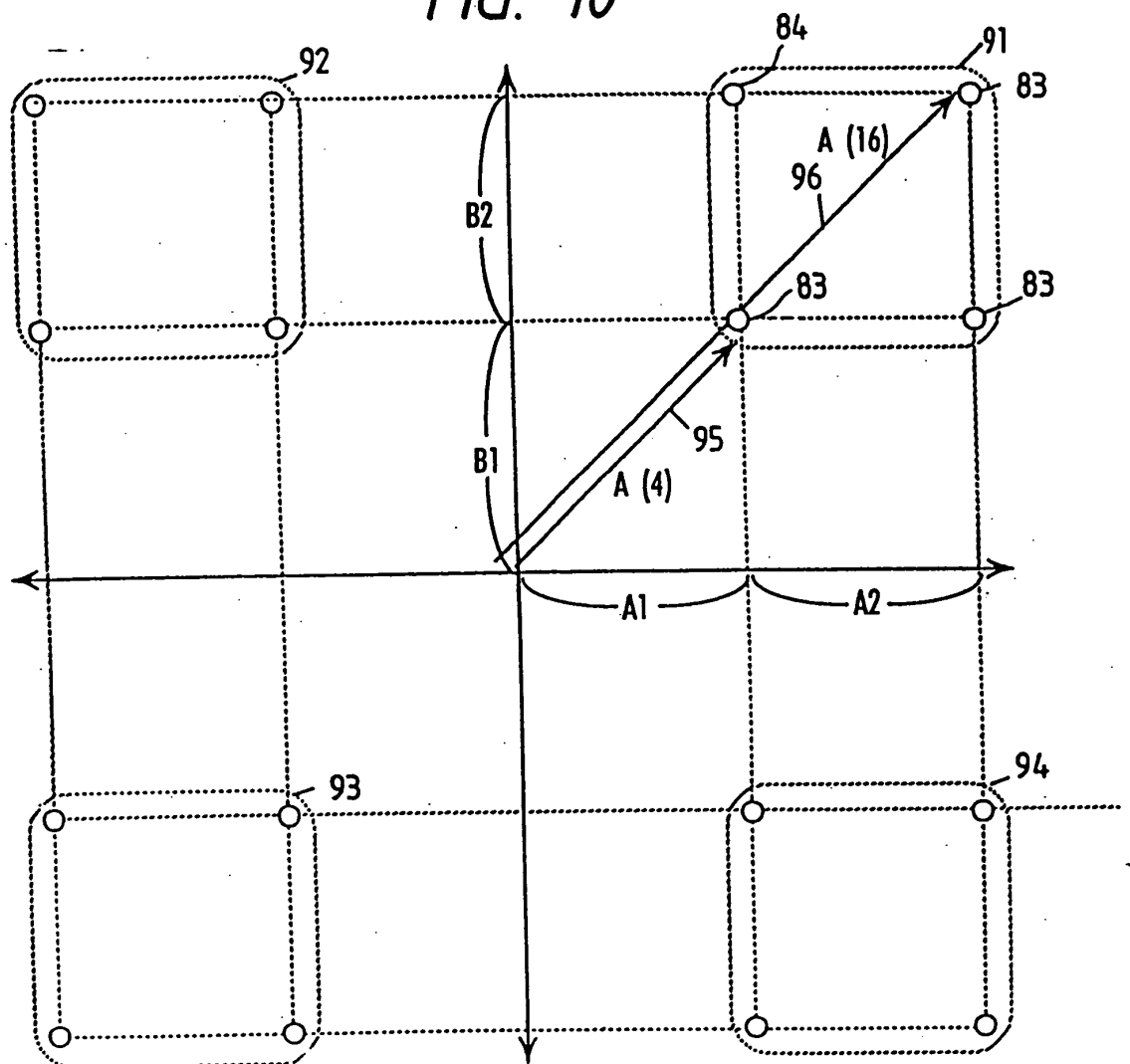


FIG. 11

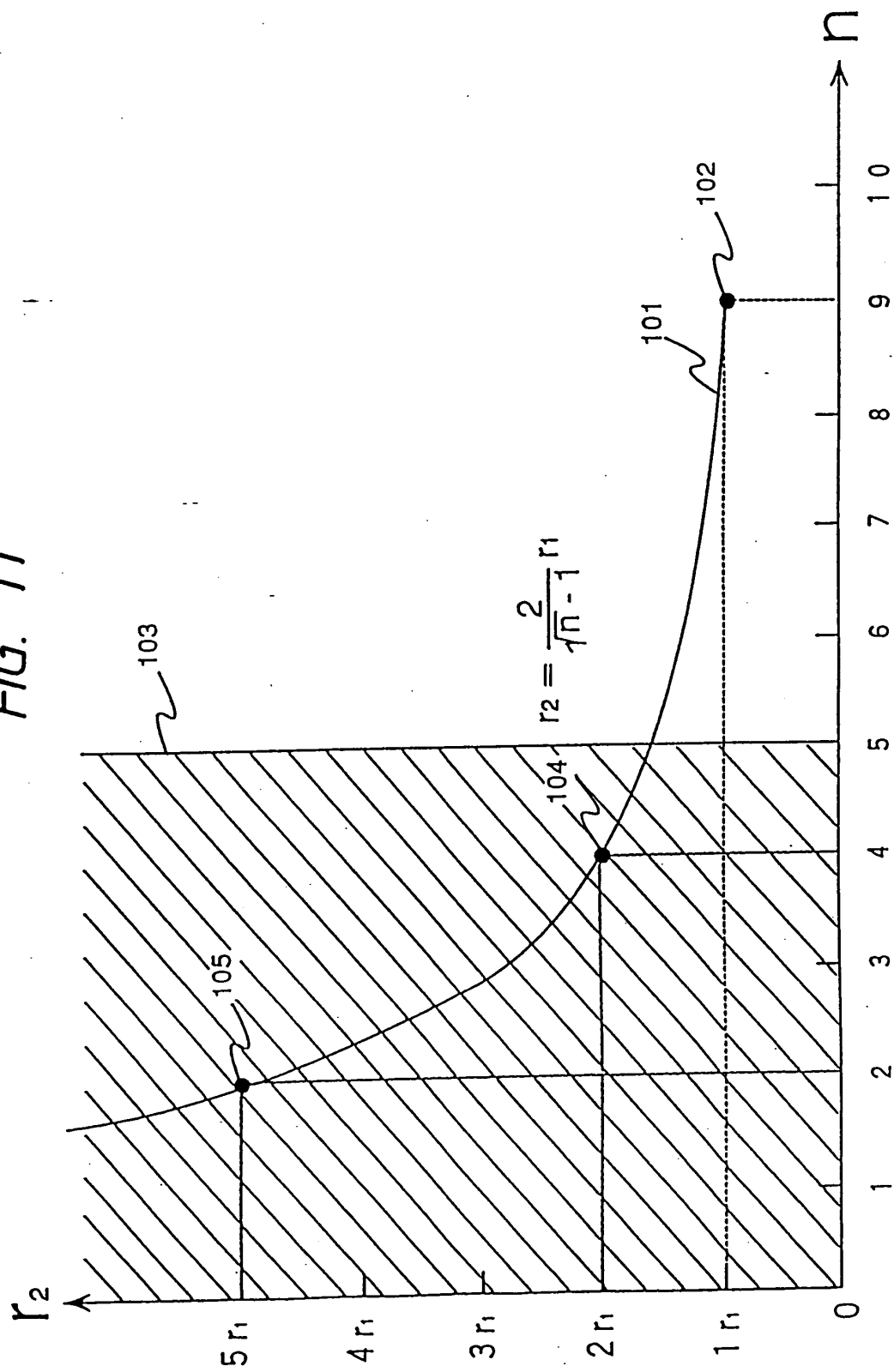


FIG. 12

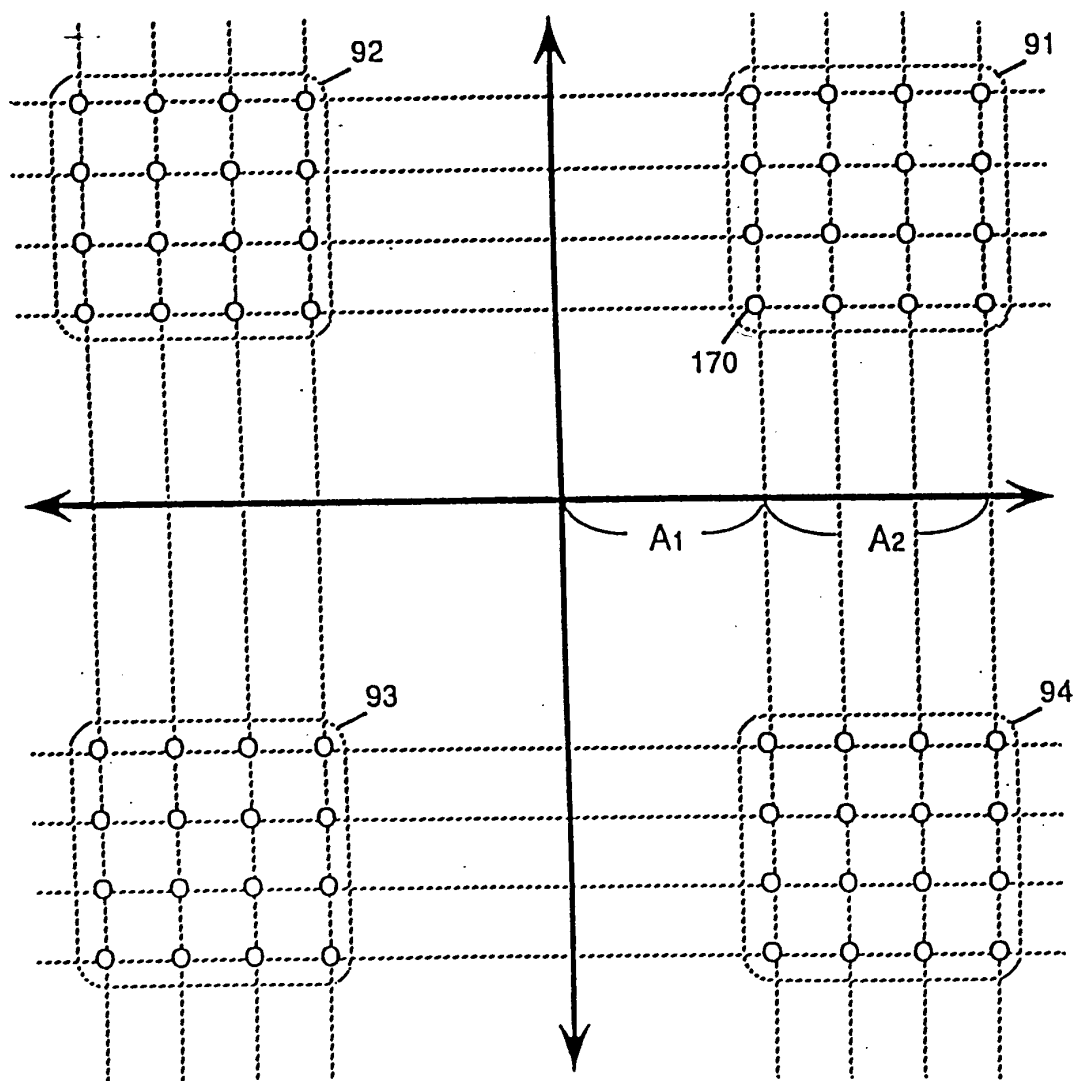


FIG. 13

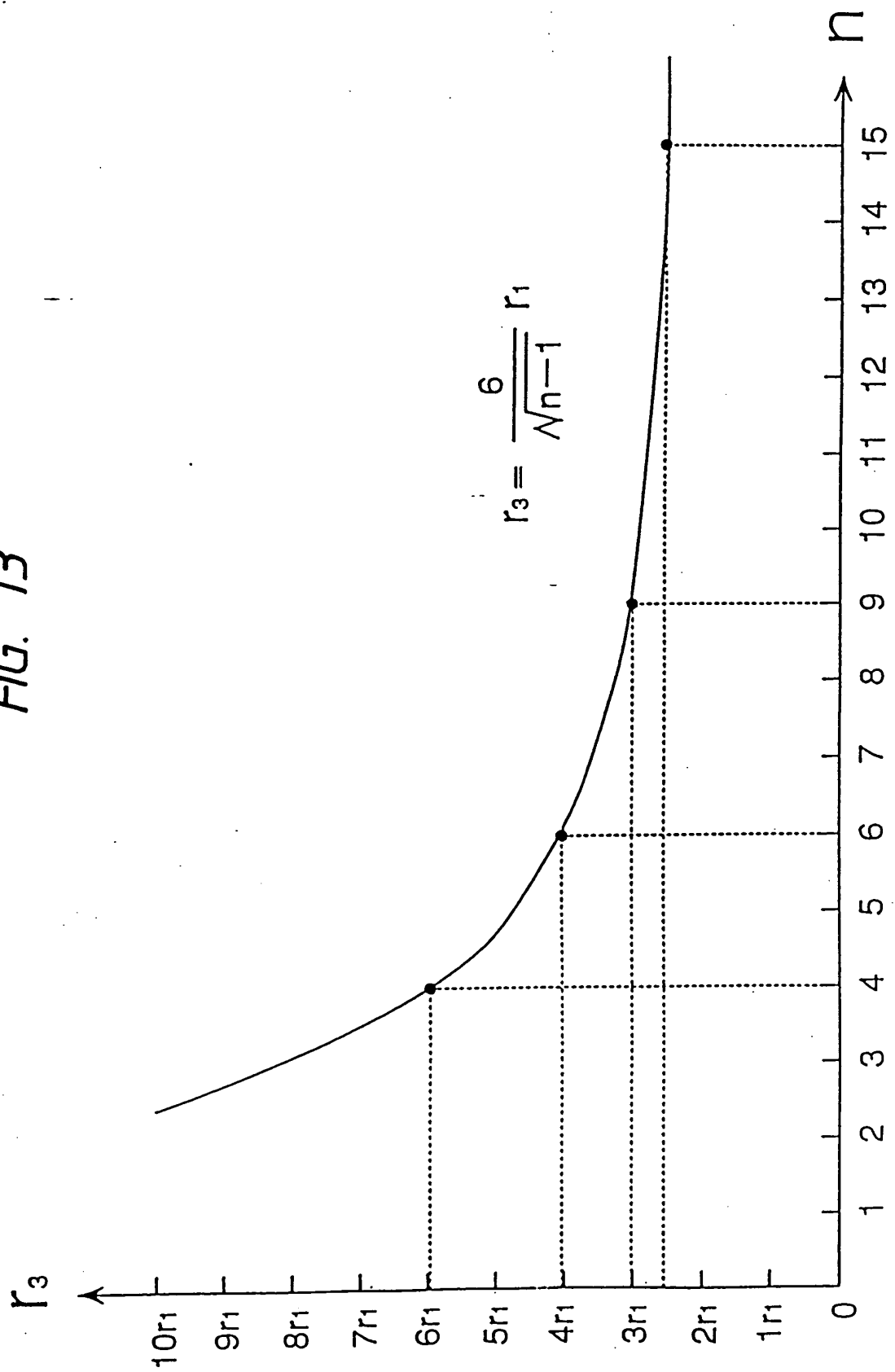
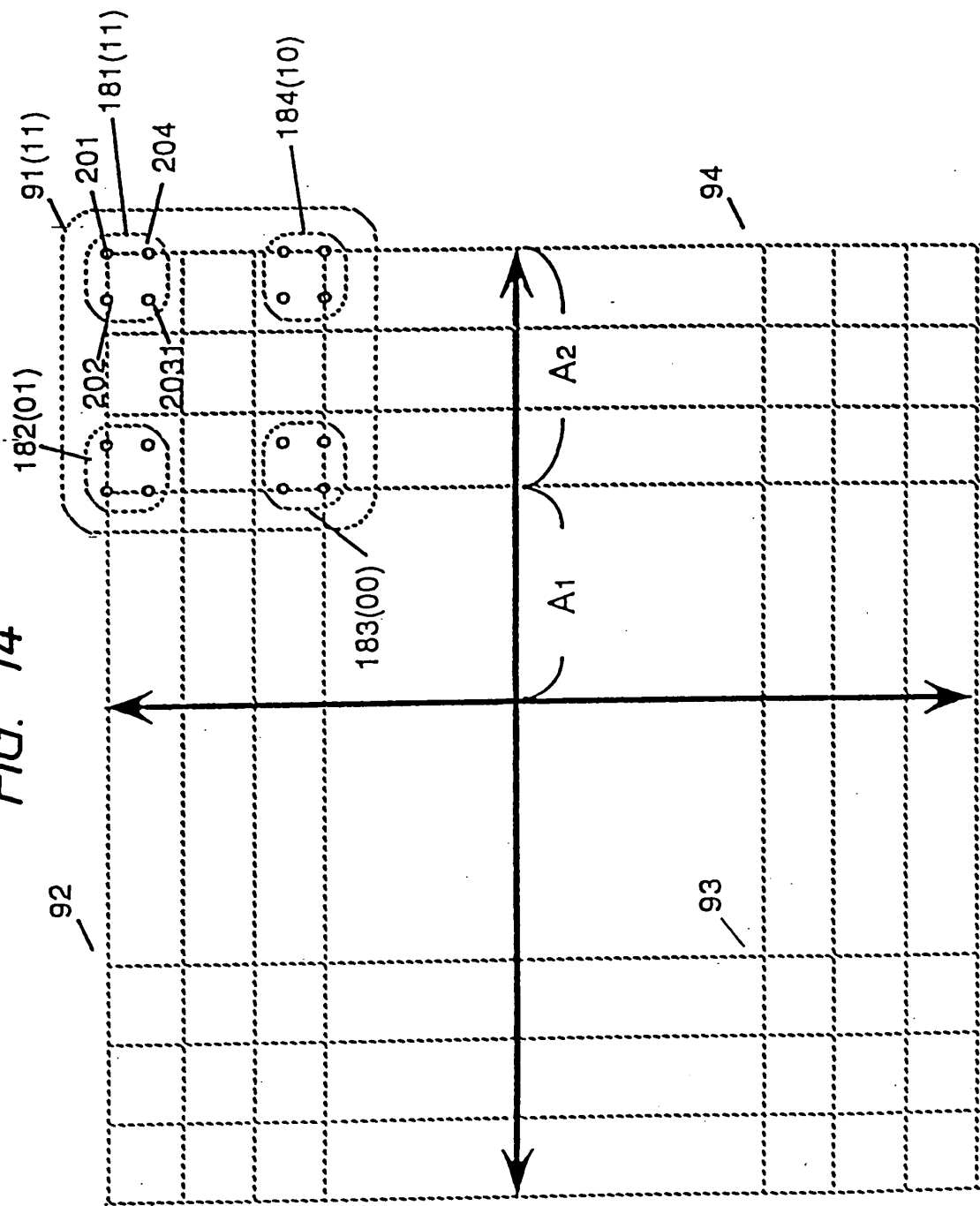


FIG. 14



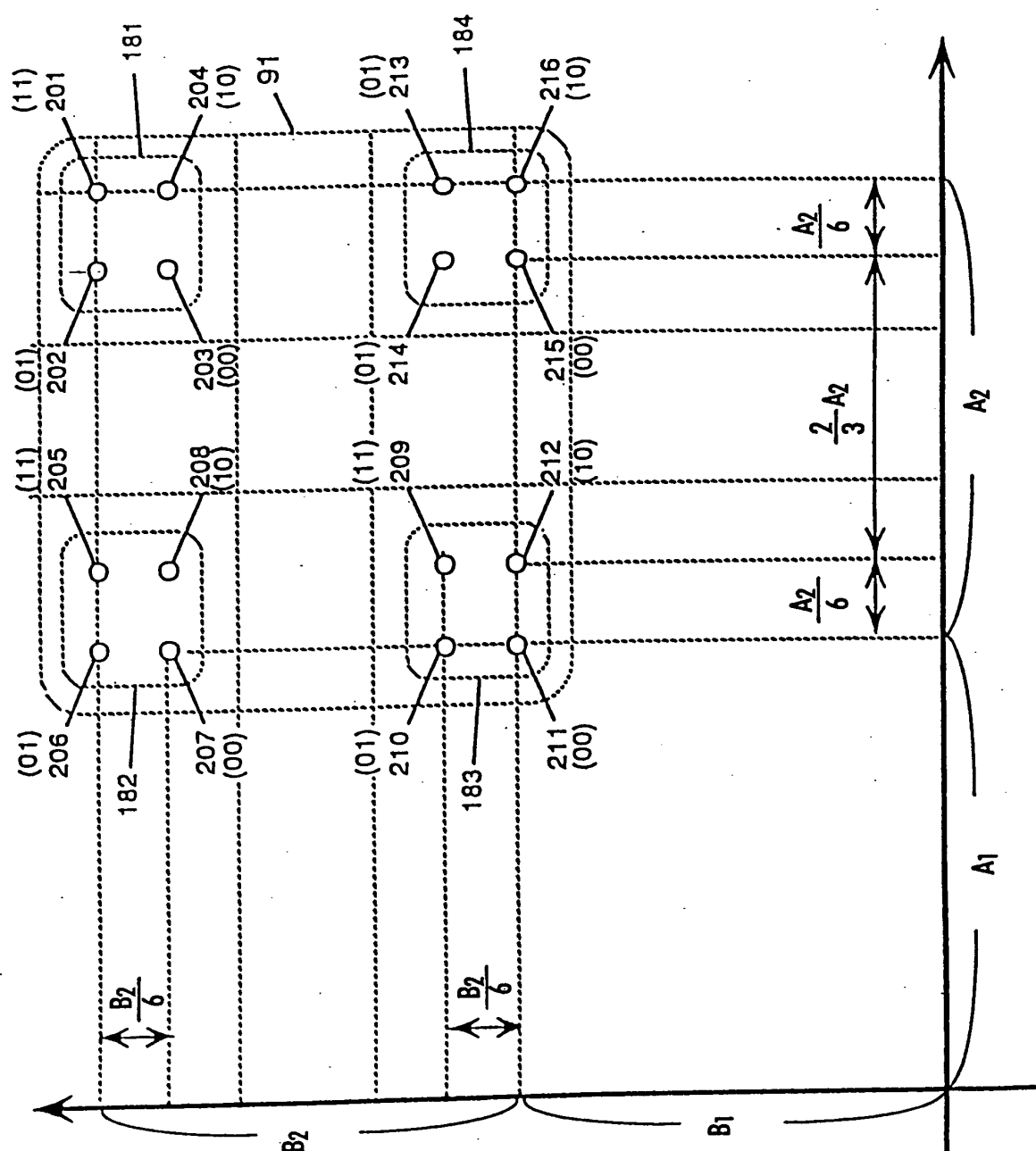


FIG. 16

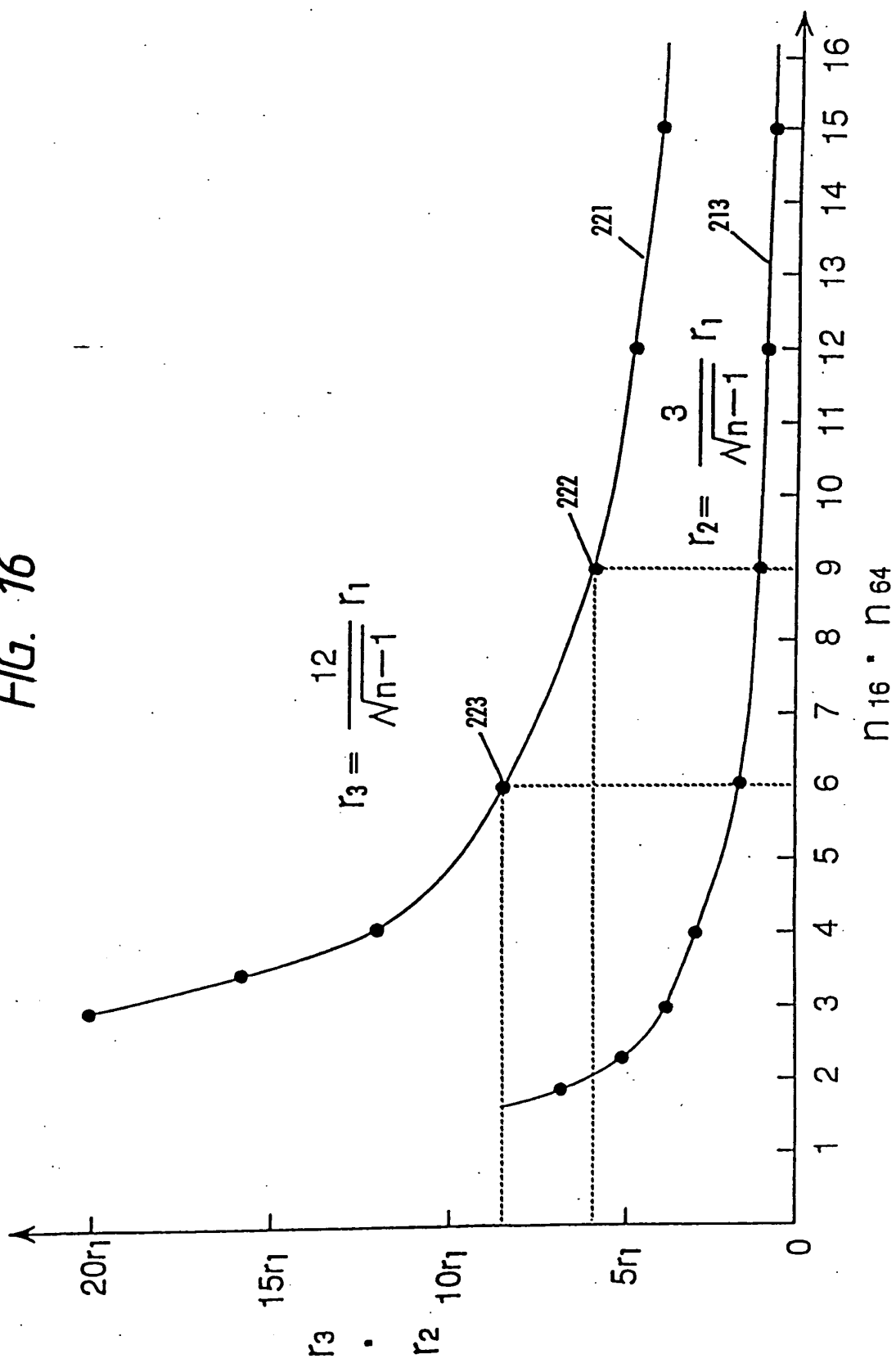


FIG. 17

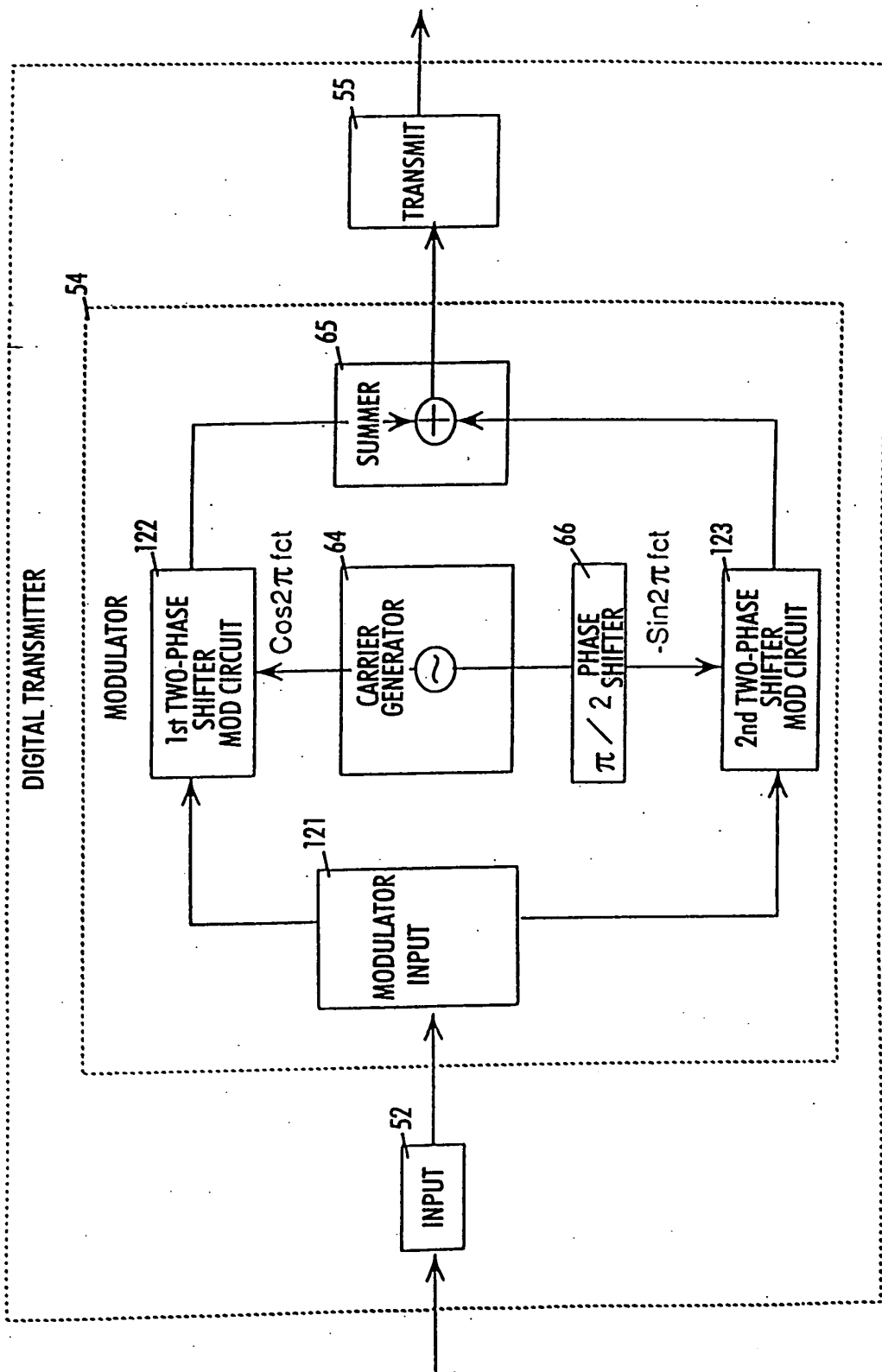


FIG. 18

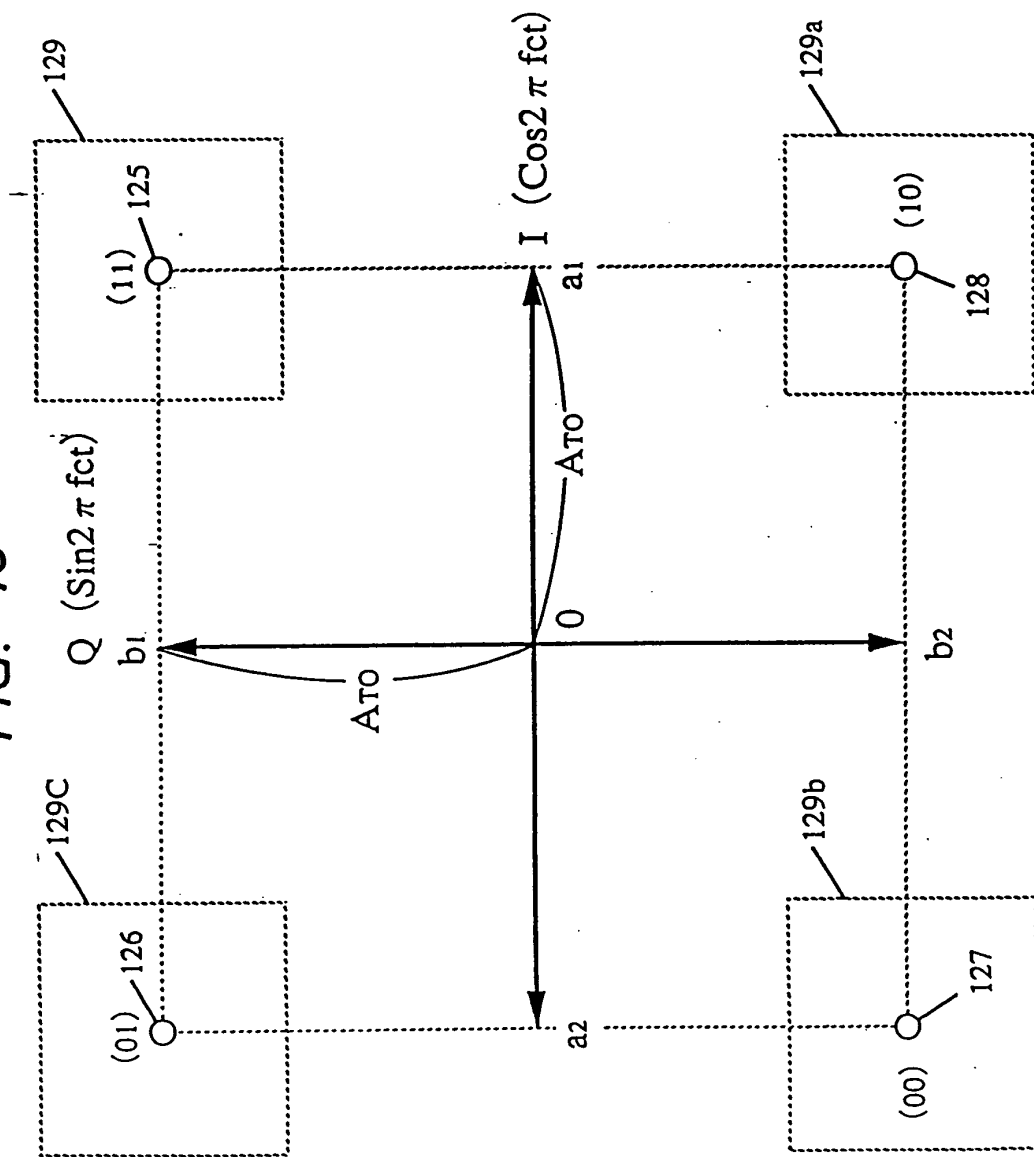


FIG. 19

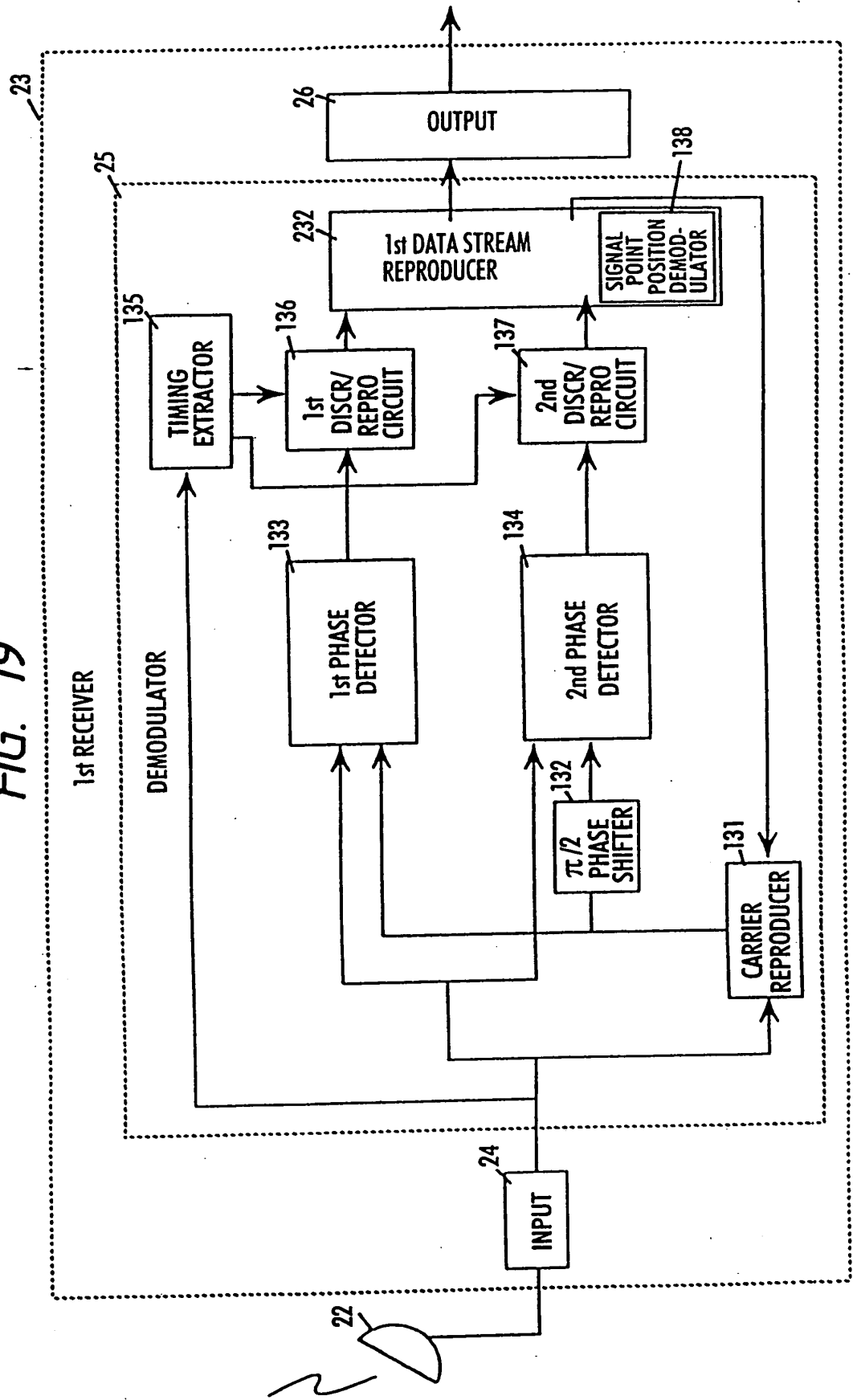


FIG. 20

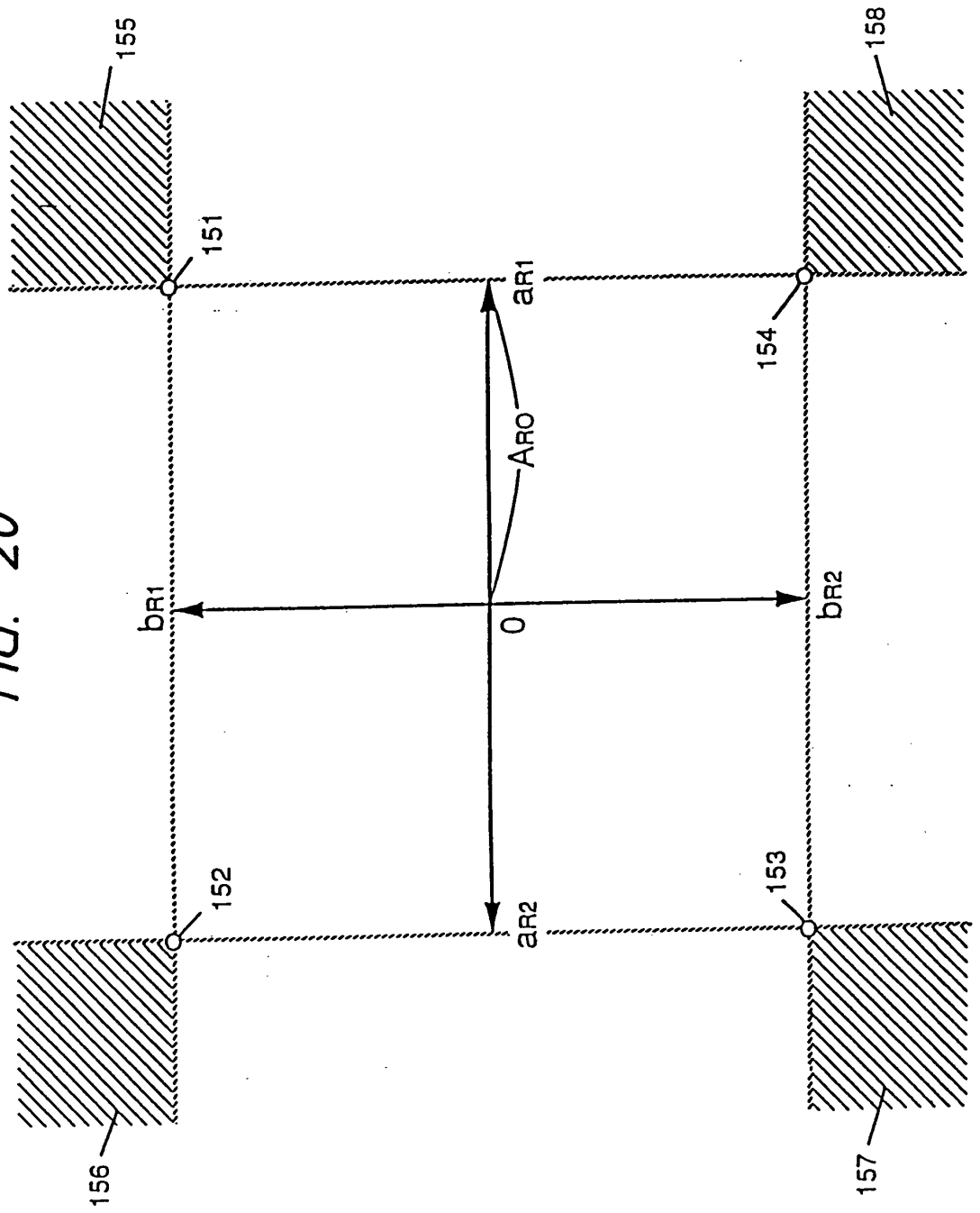


FIG. 21

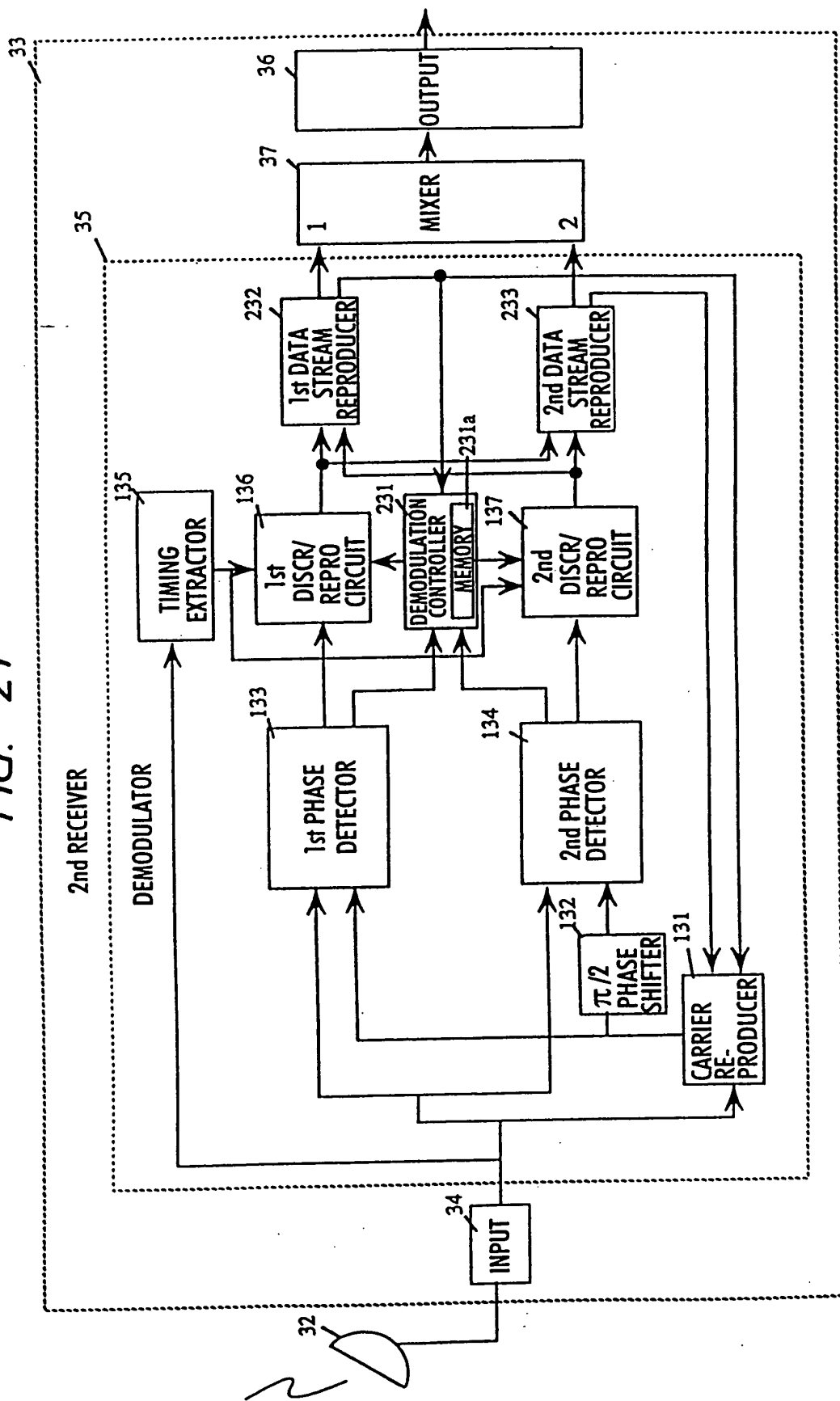
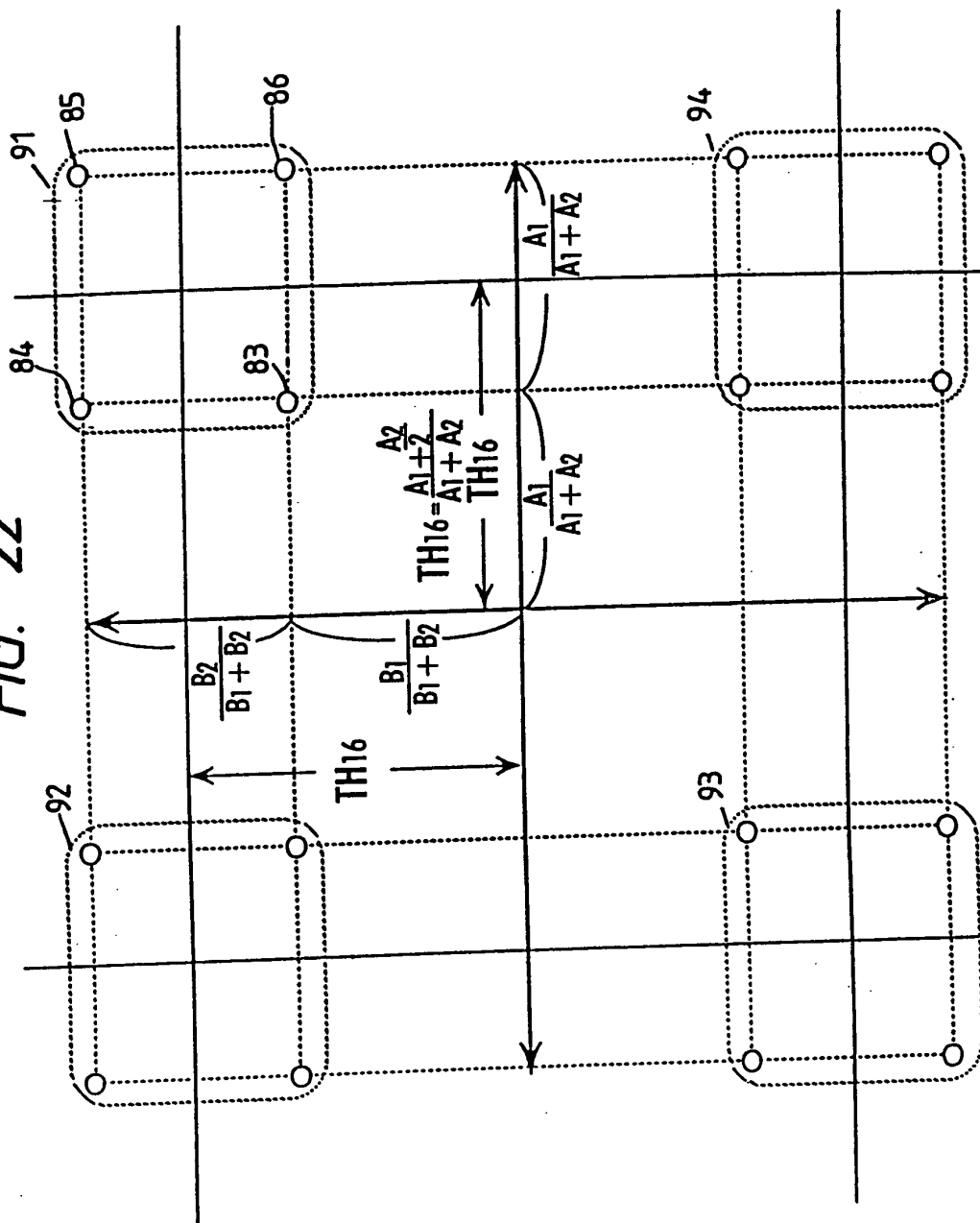


FIG. 22



23

Diagram illustrating a grid structure with nodes and dimensions. The grid is defined by dashed lines. Nodes are labeled with numbers: 201, 202, 203, 204, 205, 206, 207, 208, 209, 210, 211, 212, 213, 214, 215, 216. Dimensions are indicated by arrows: A1 (width), A2 (height), A3 (small segment), B1 (width), B2 (height). The diagram shows a grid of nodes connected by dashed lines, with some nodes grouped by brackets. The overall dimensions are A1 and A2, and the grid is divided into sections B1 and B2. The diagram is labeled 23 in the top left corner.

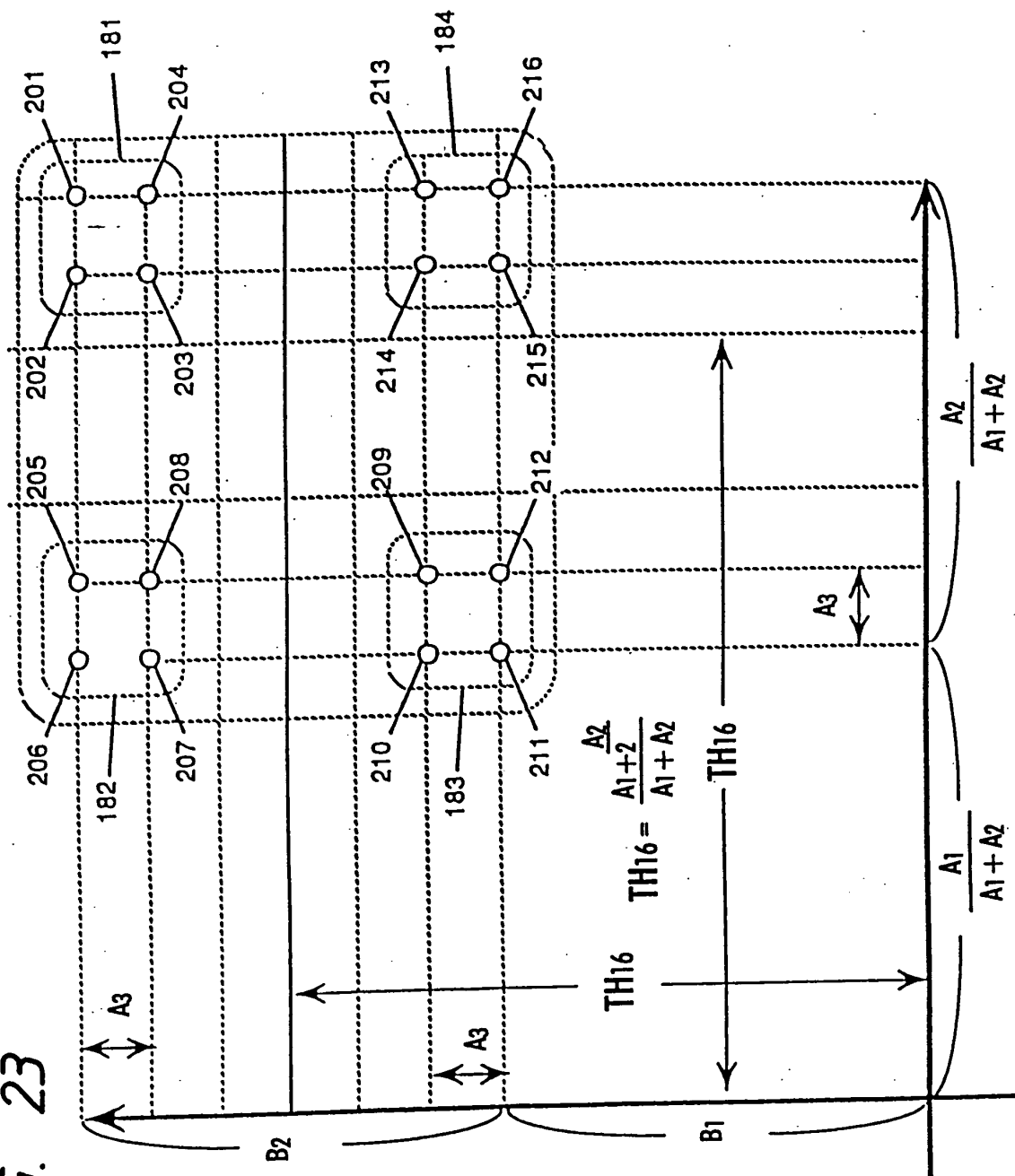


FIG. 24

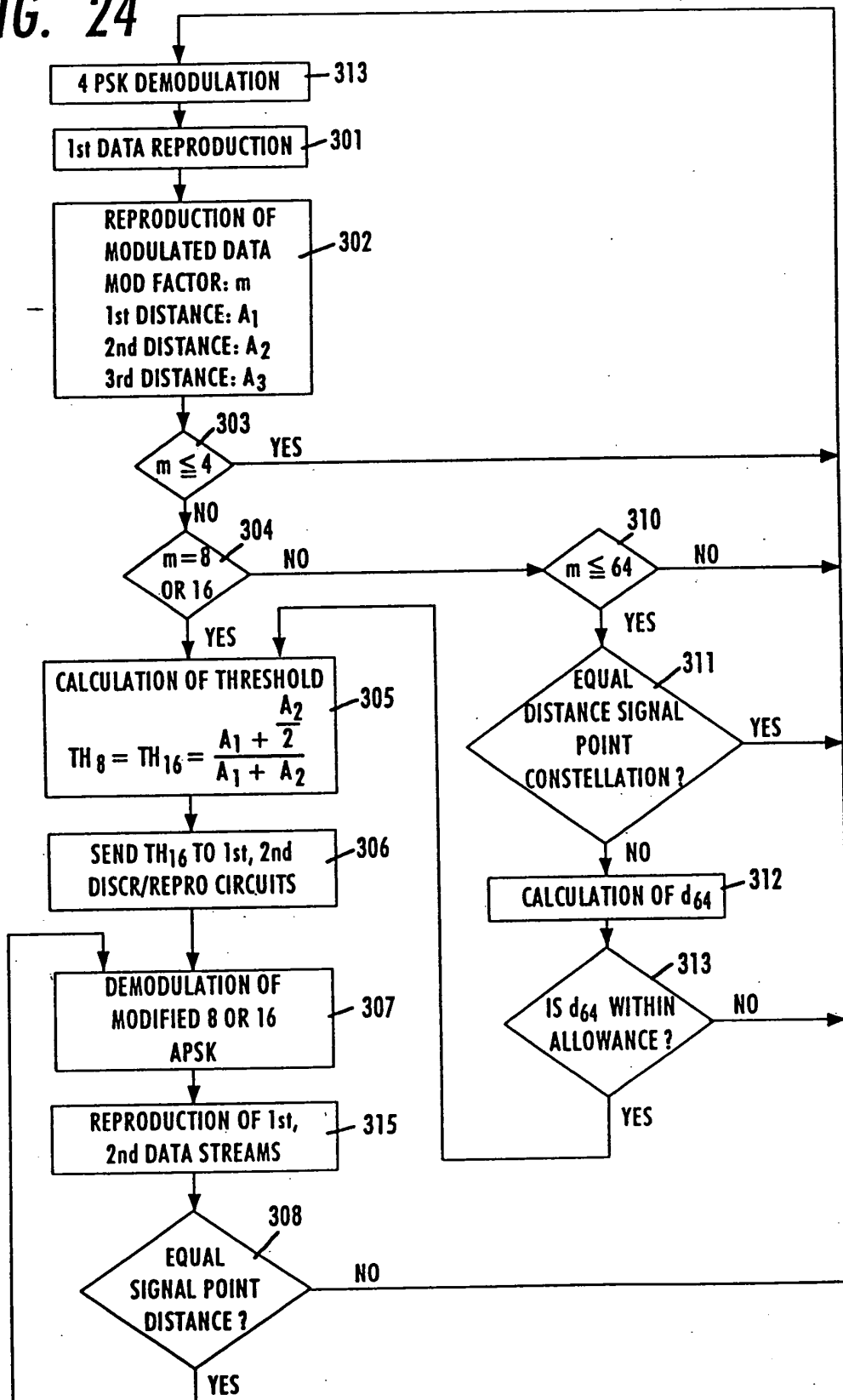


FIG. 25(A)

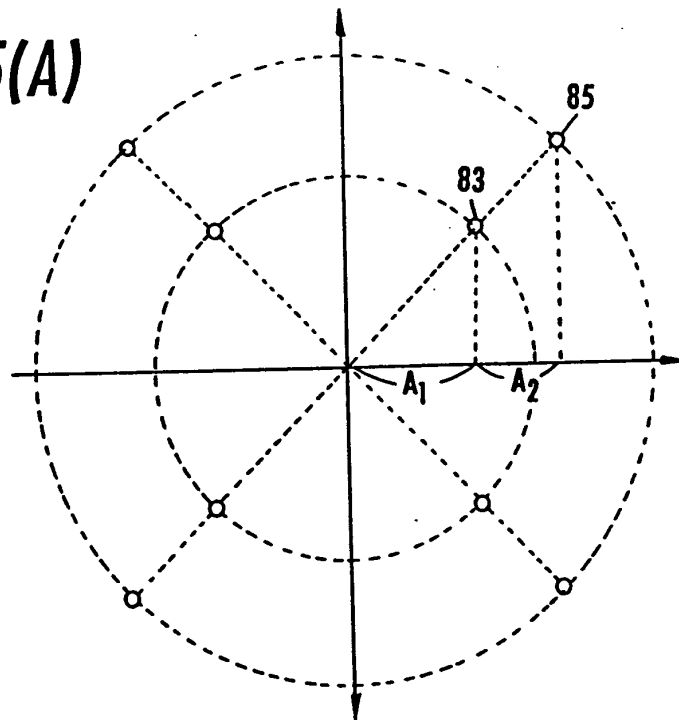


FIG. 25(B)

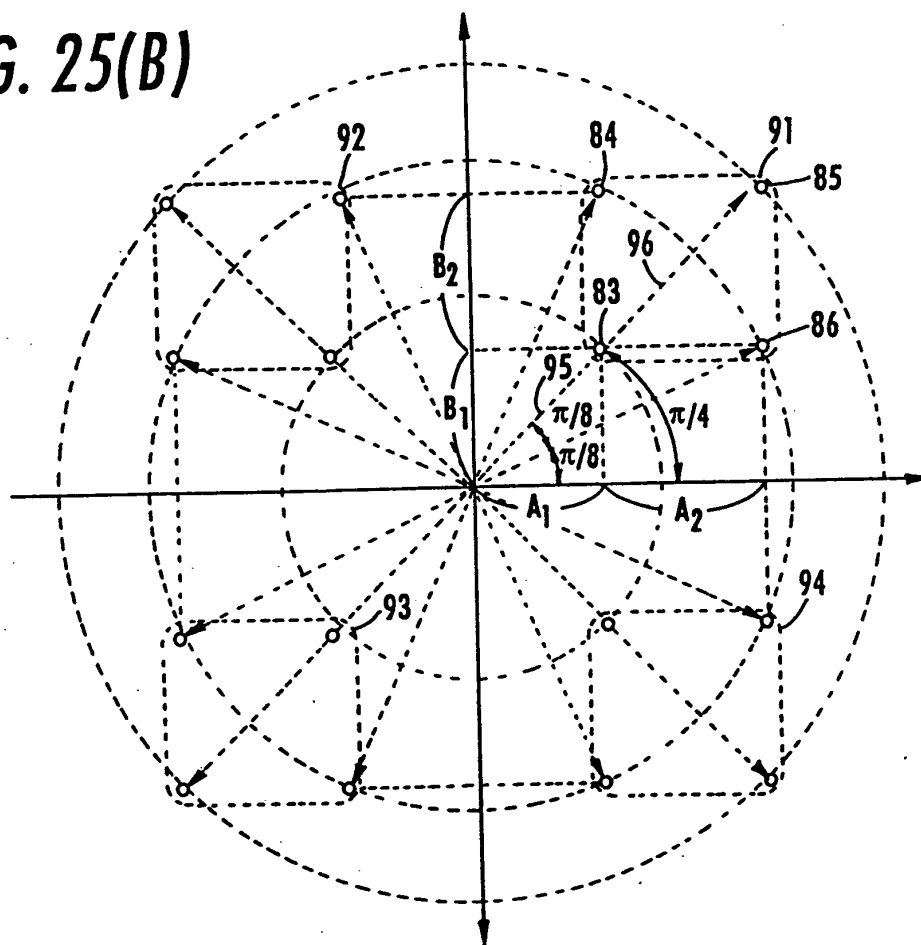
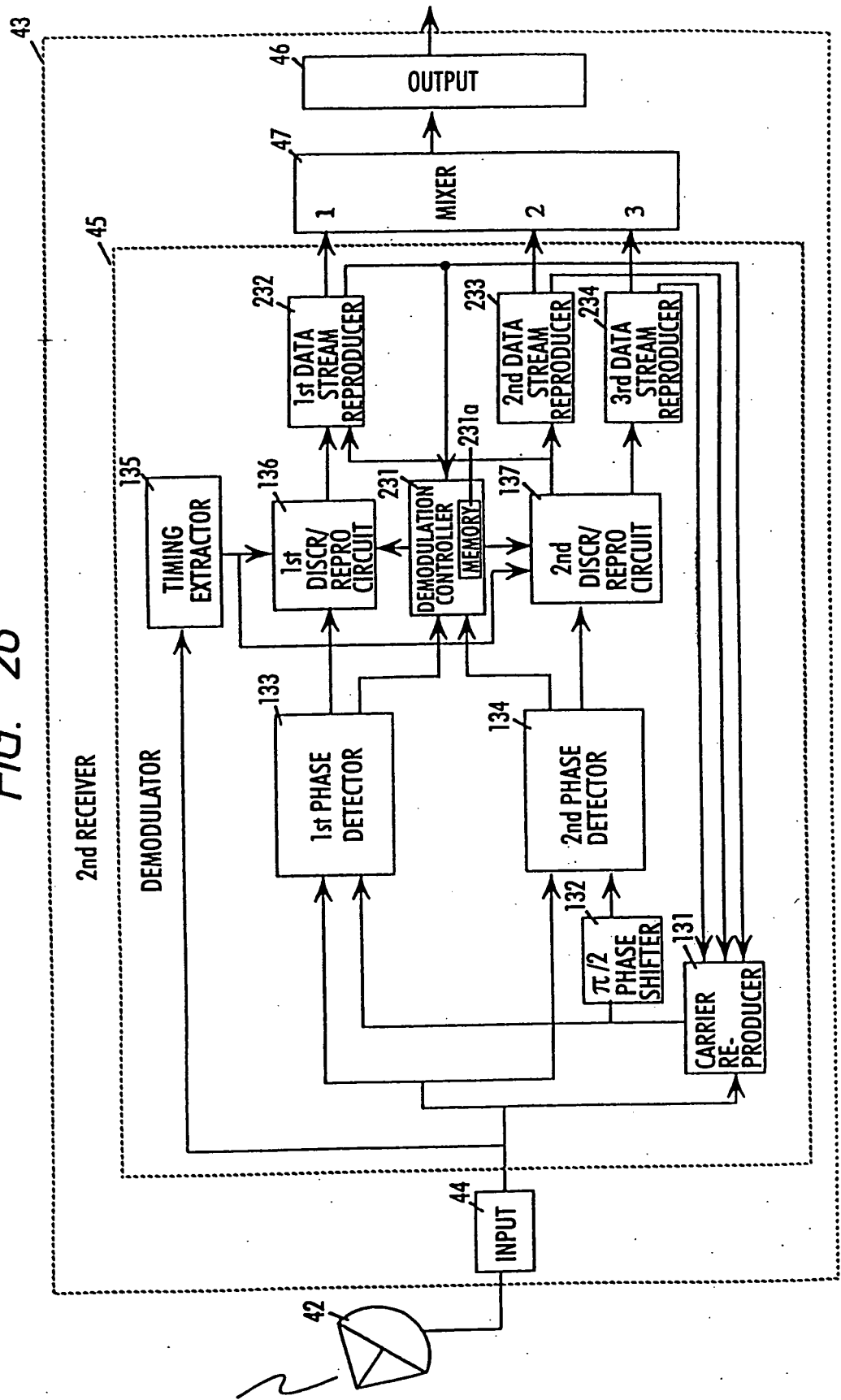
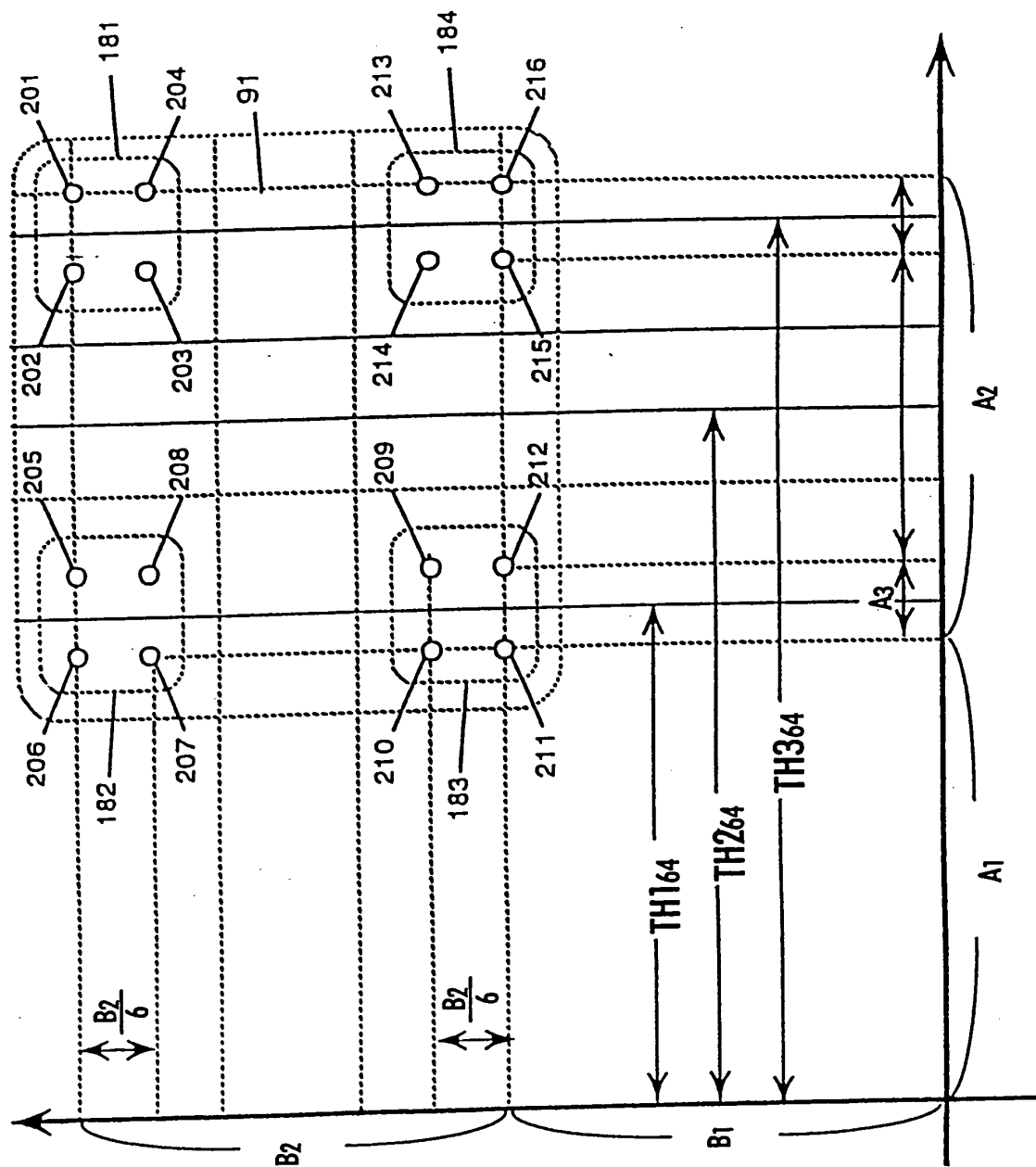


FIG. 26



[illegible]

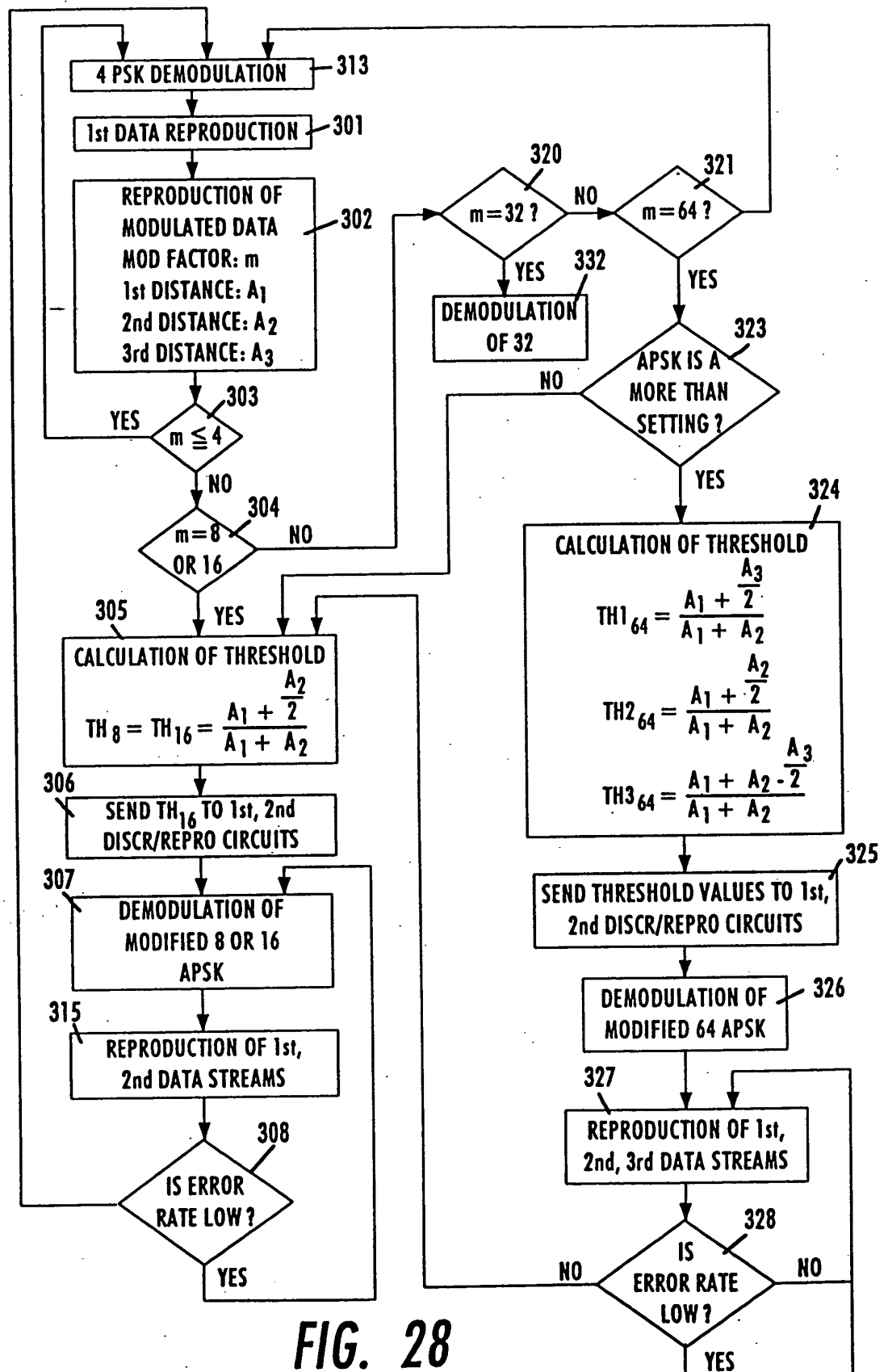


FIG. 29

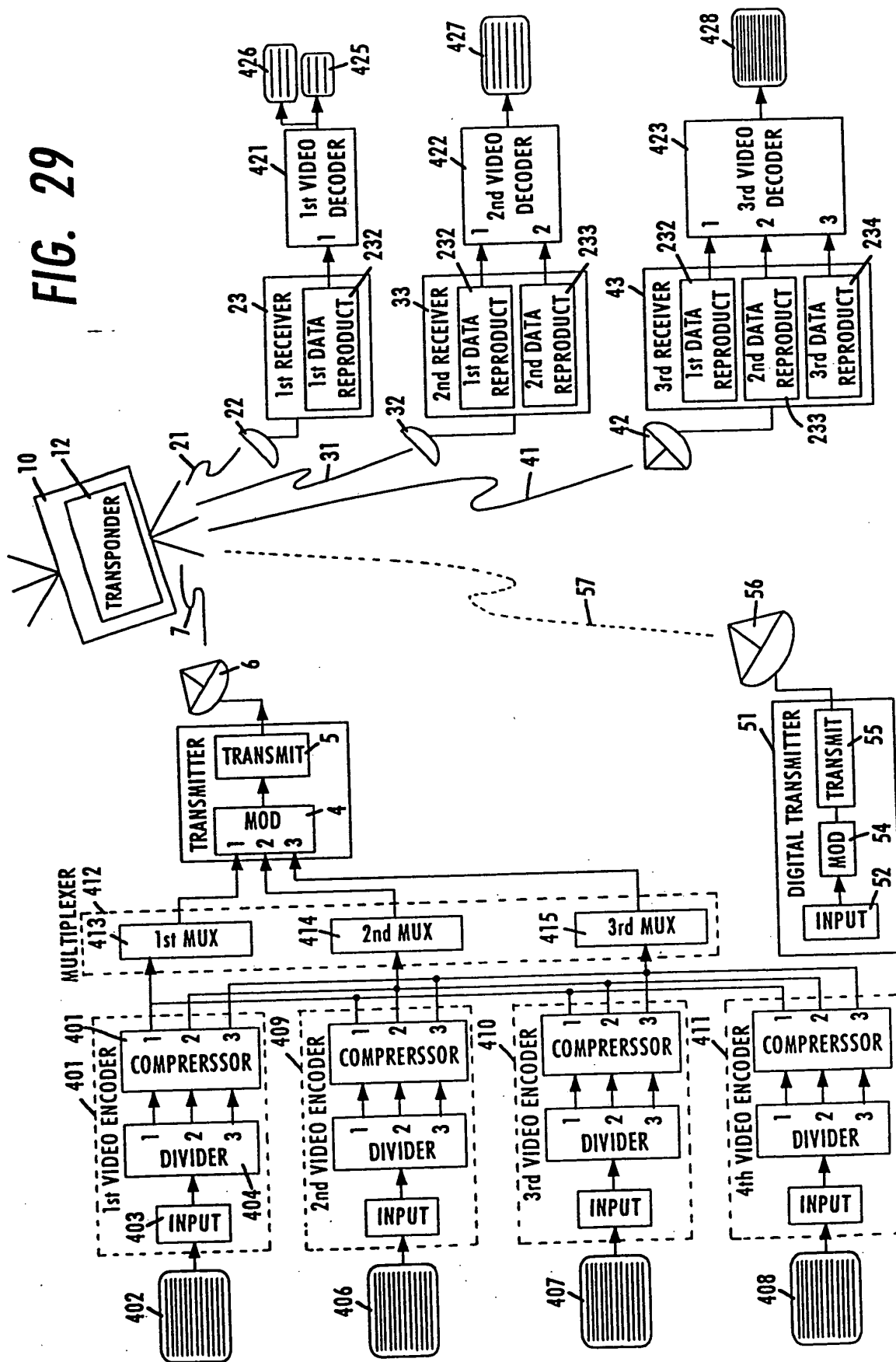


FIG. 30

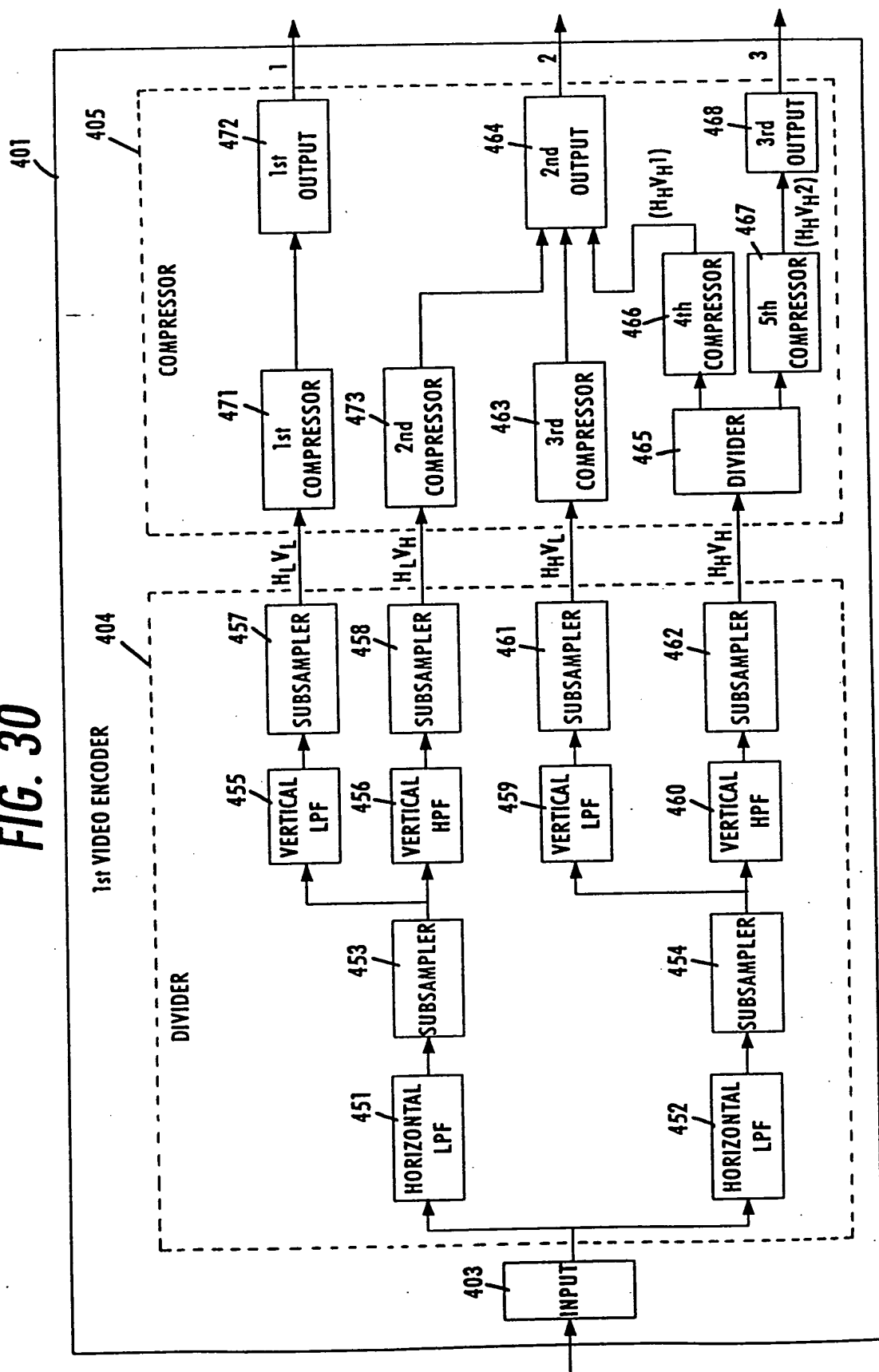


FIG. 31

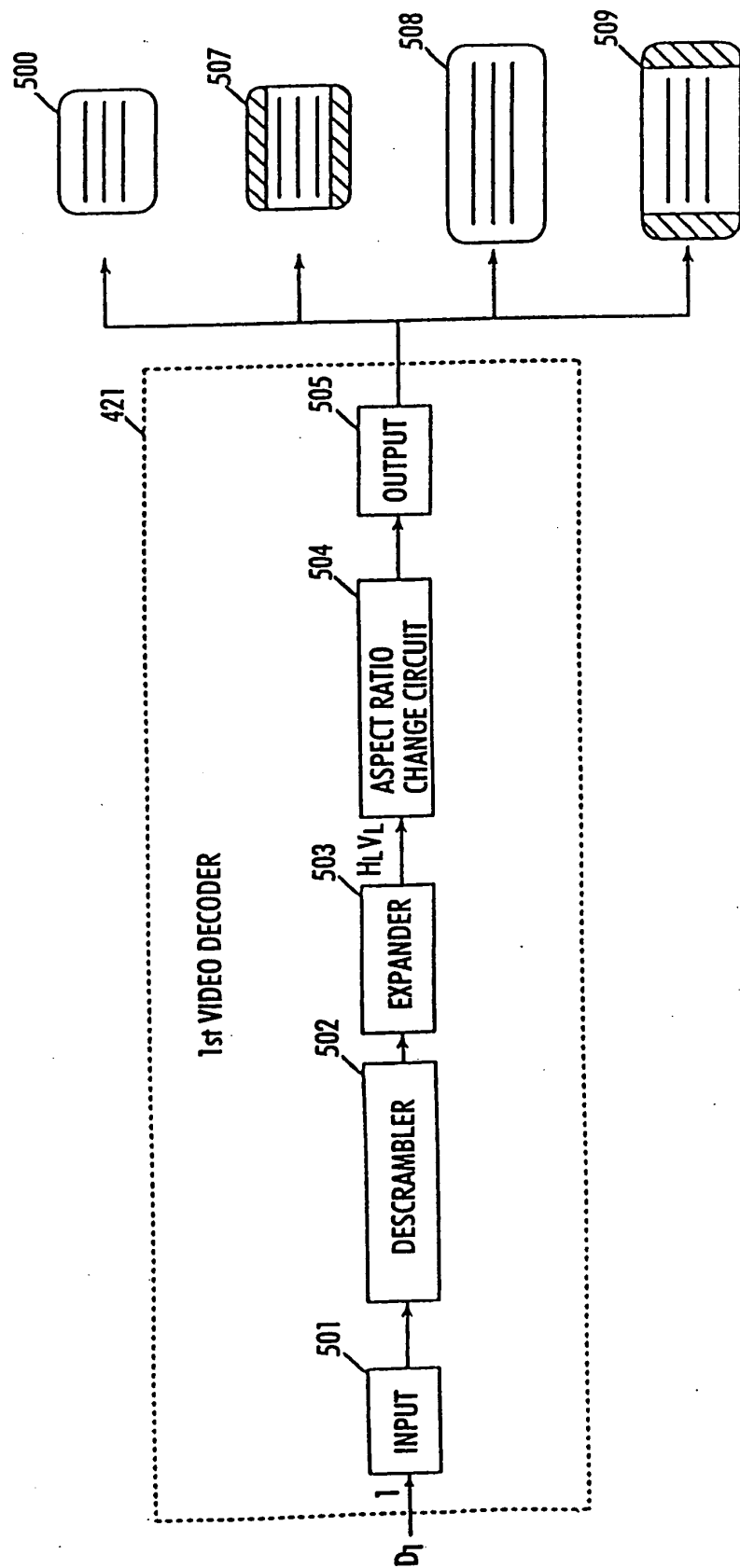


FIG. 32

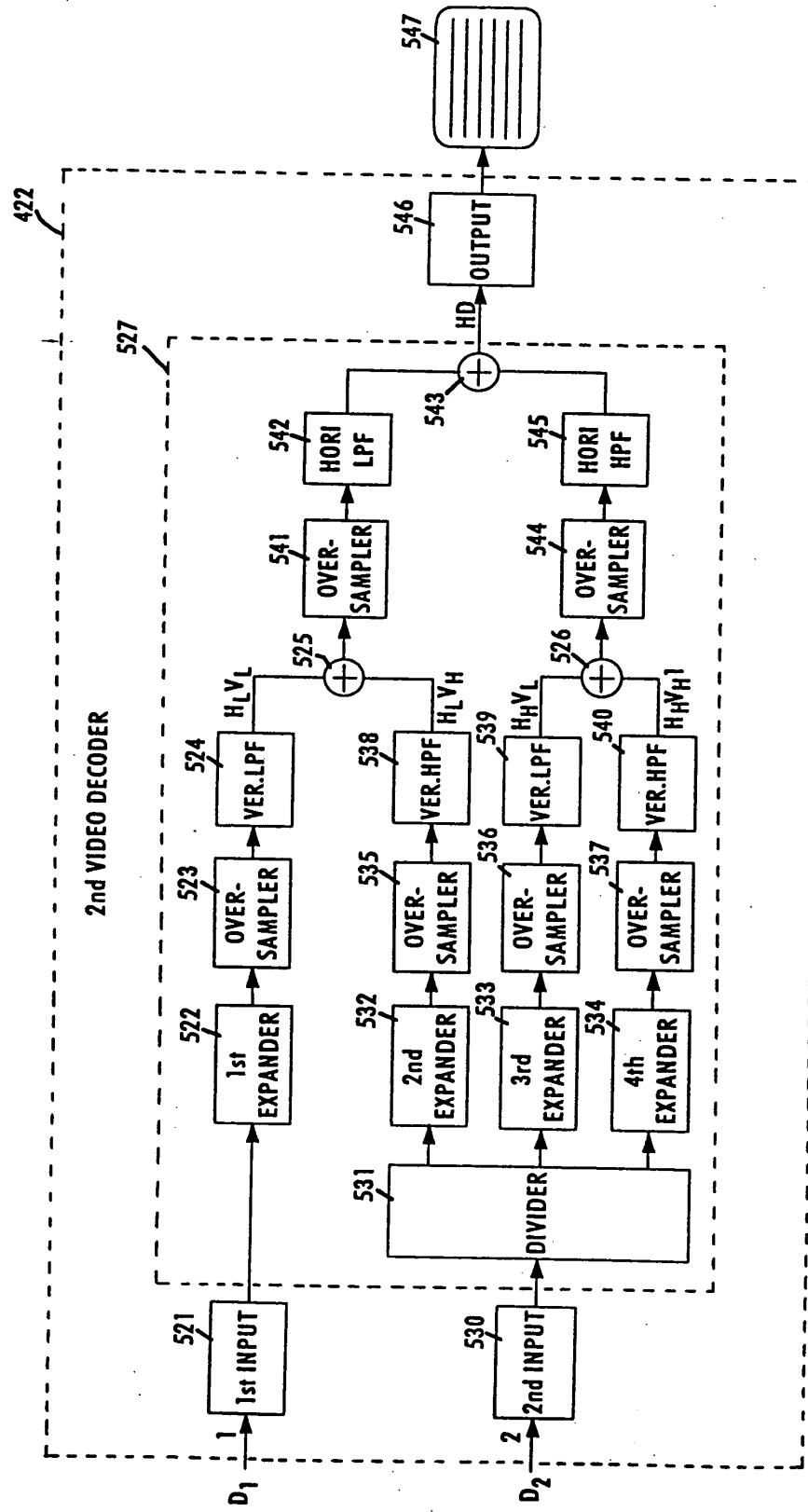


FIG. 33

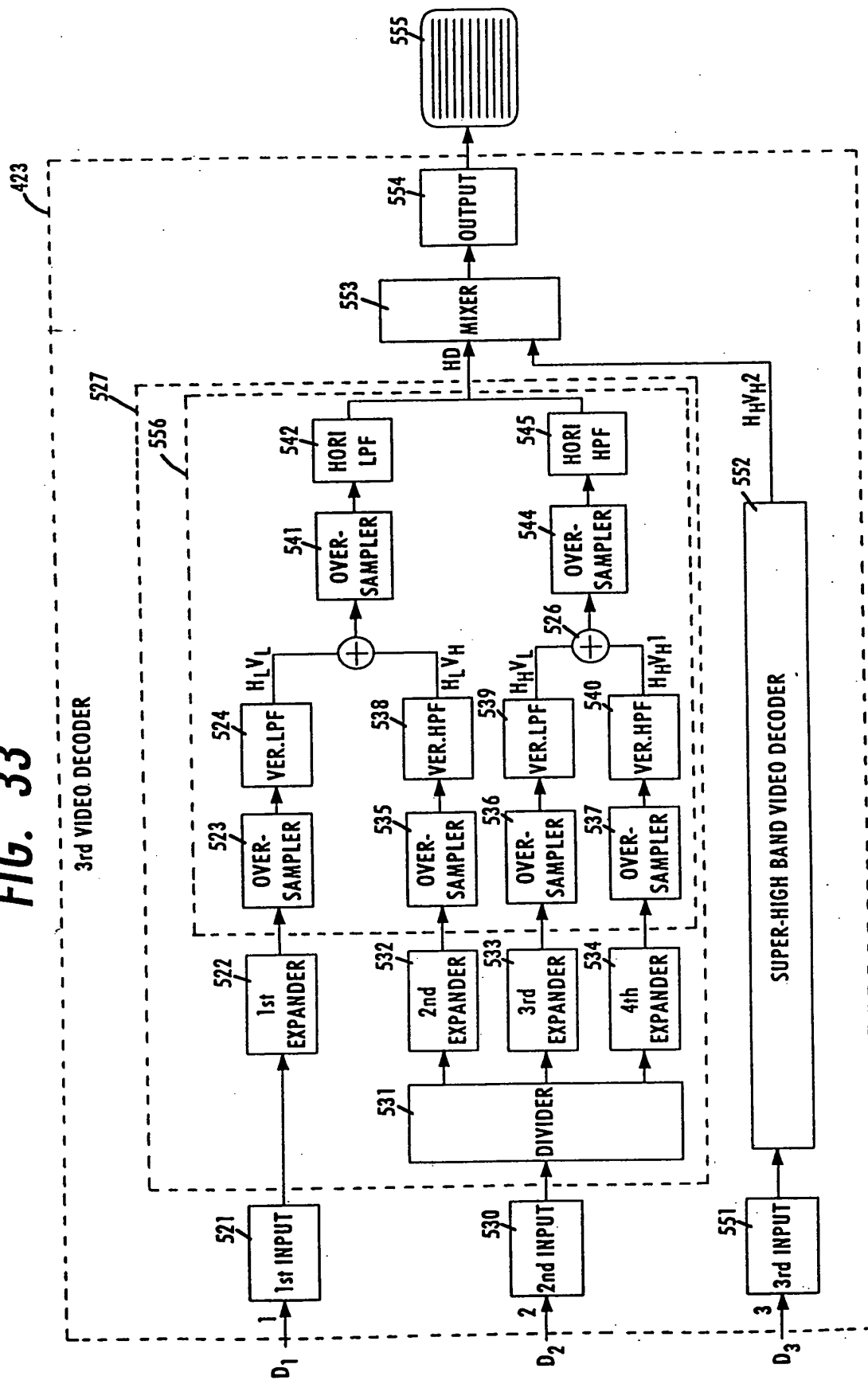


FIG. 34

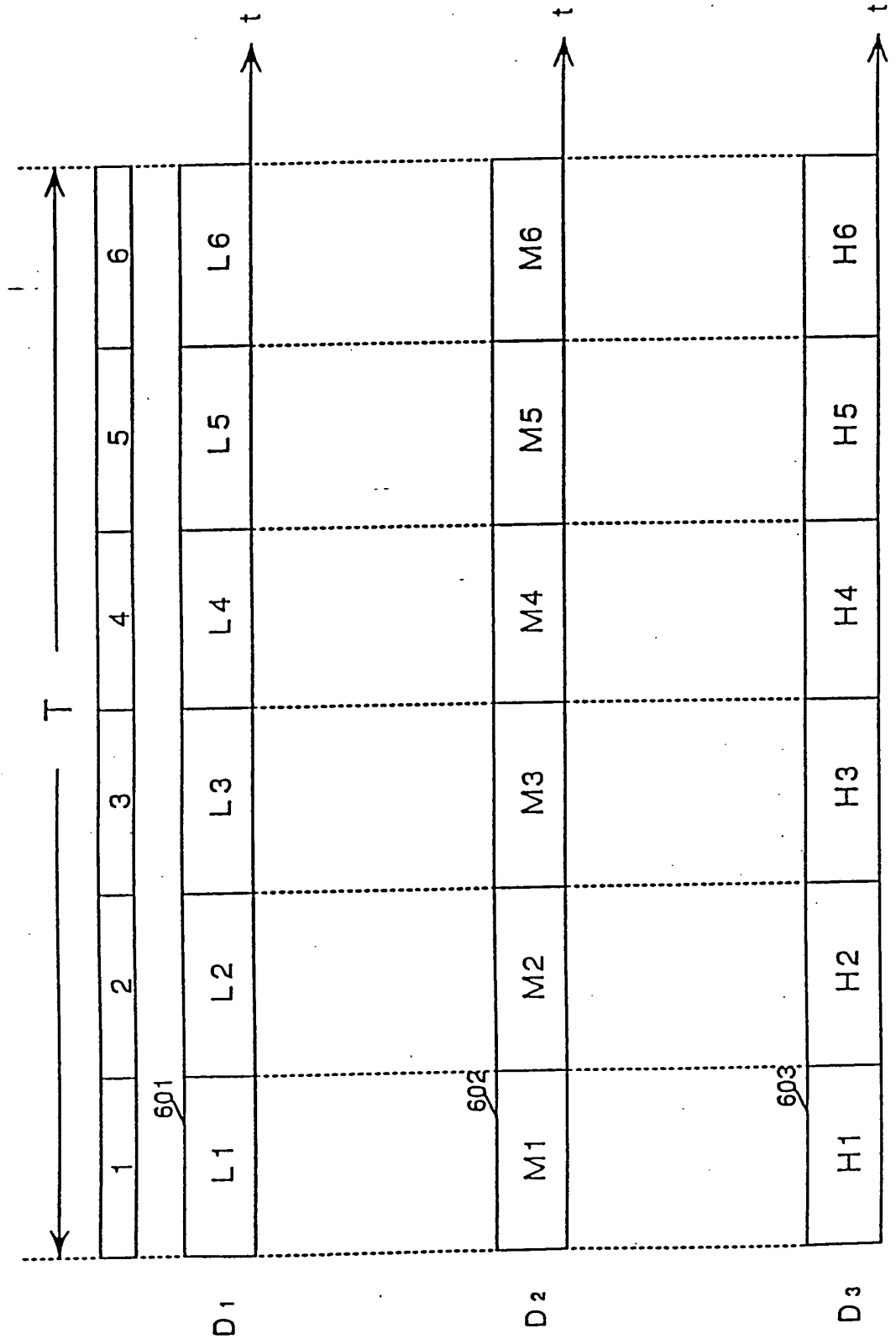


FIG. 35

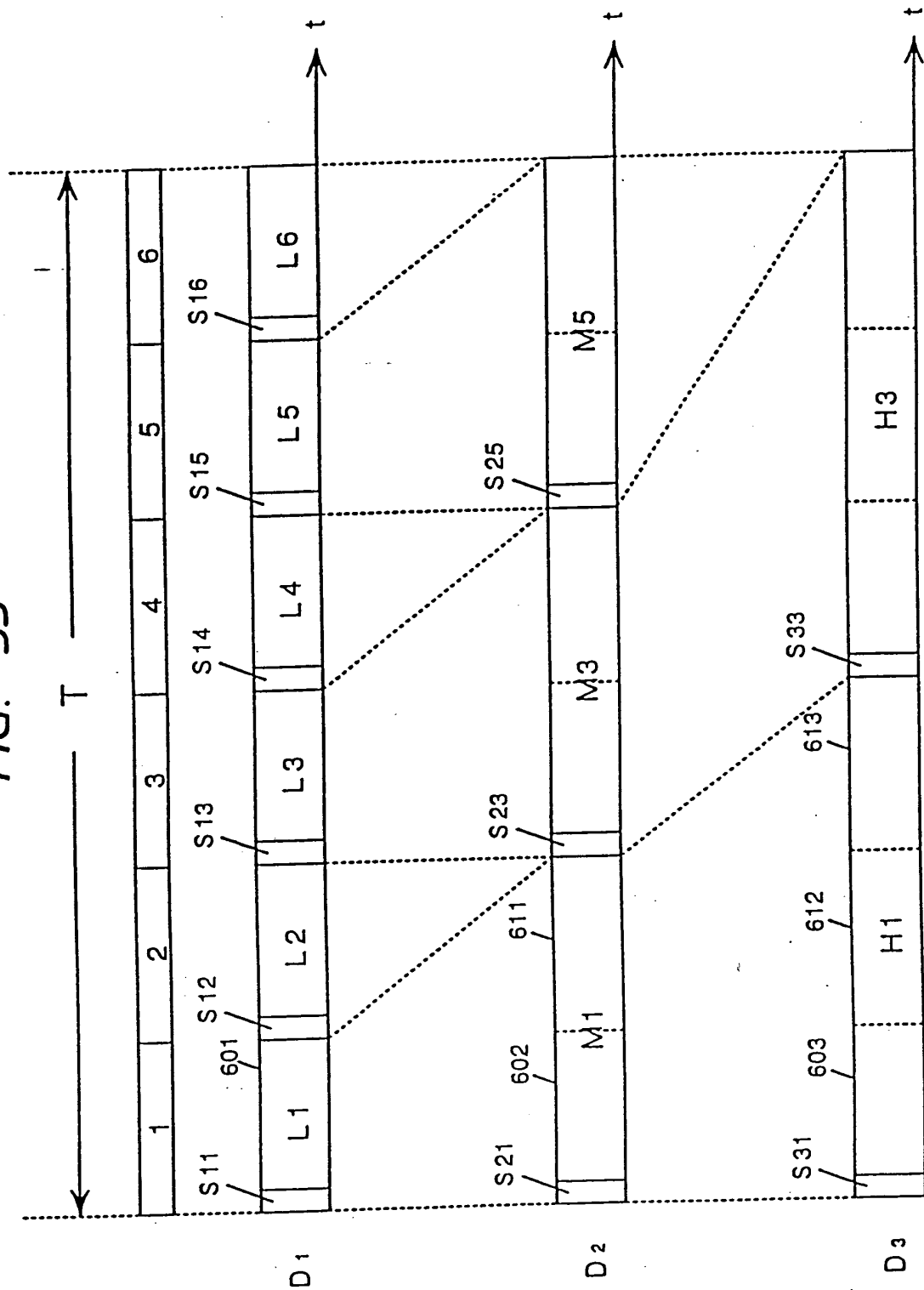


FIG. 36

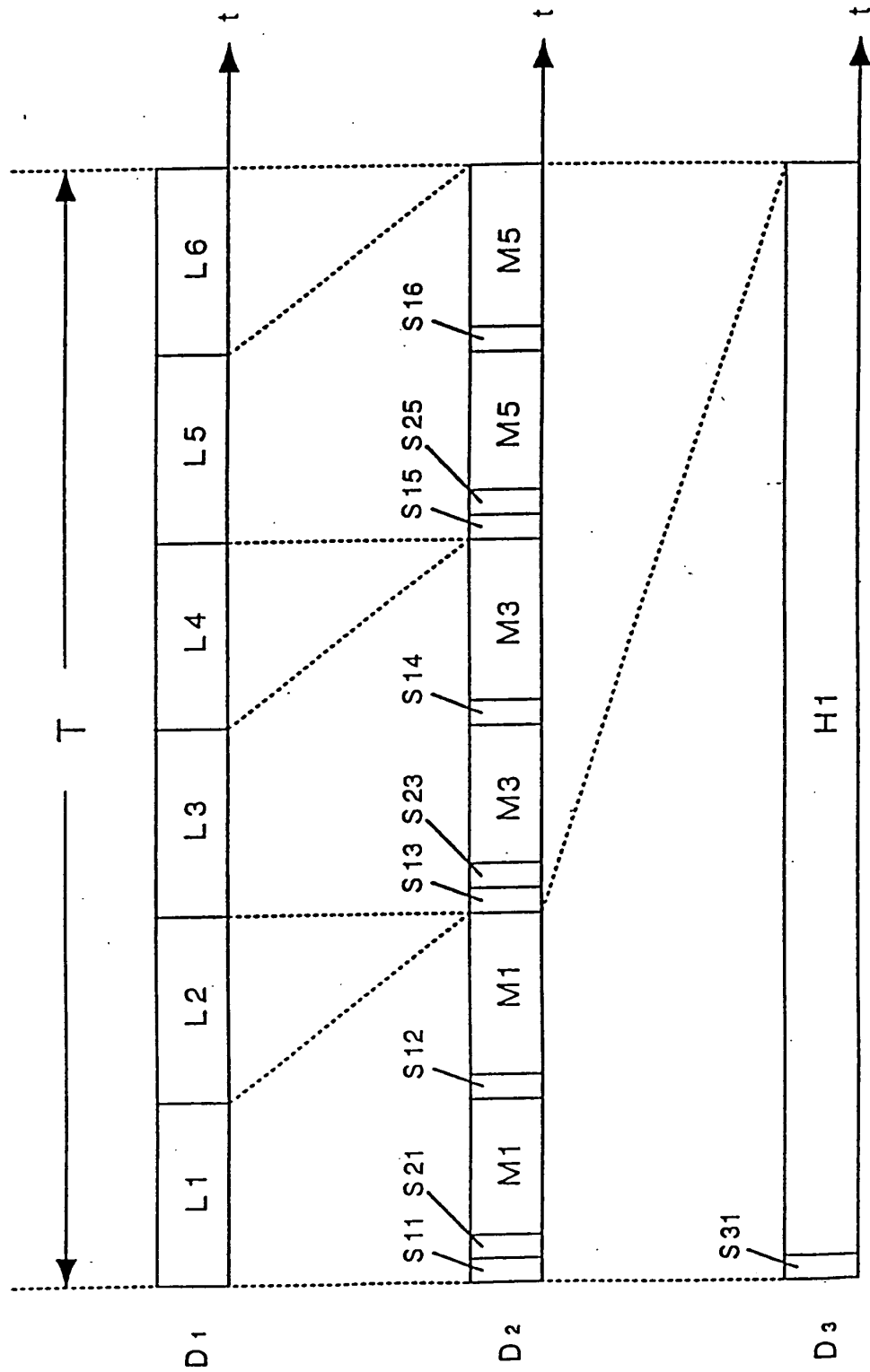


FIG. 37

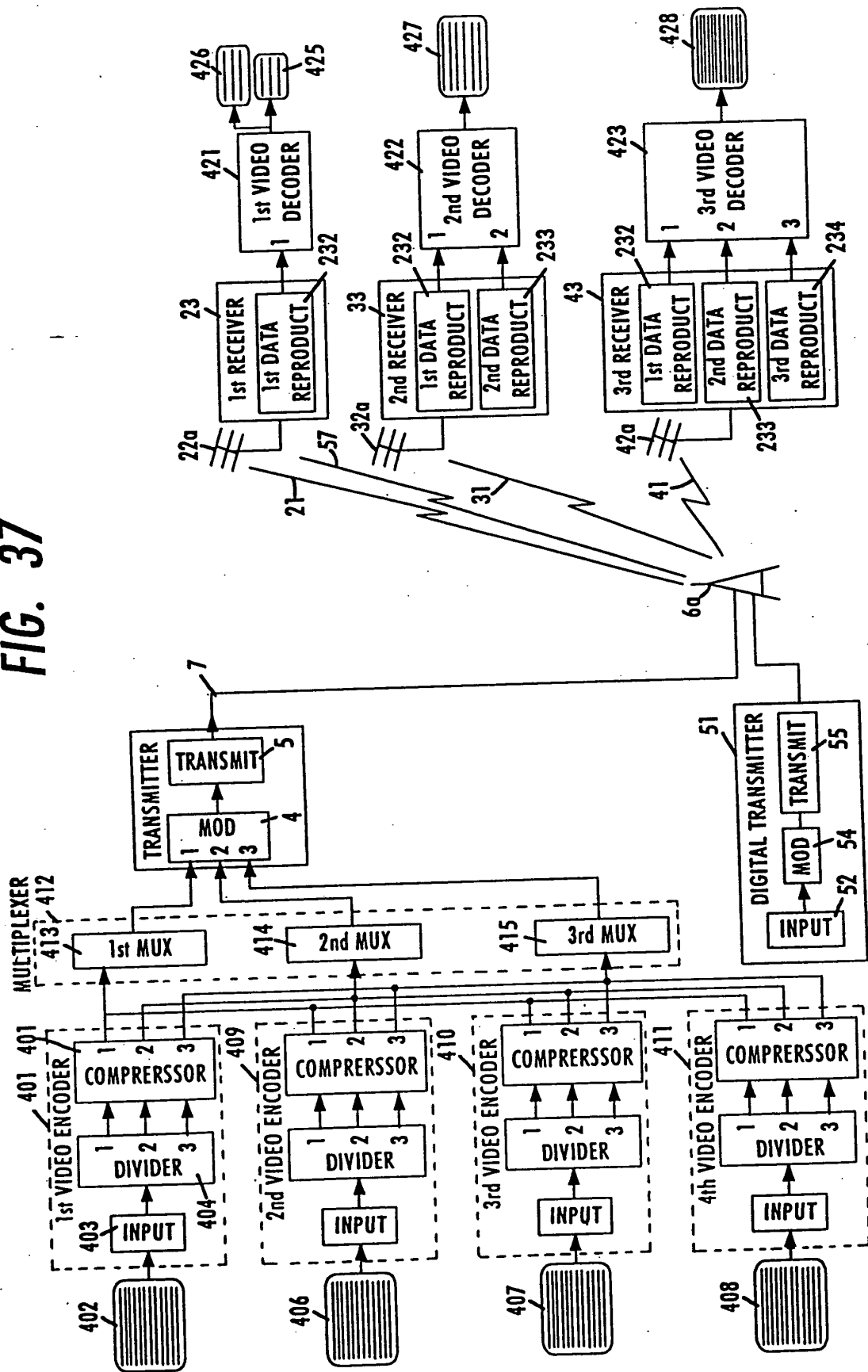
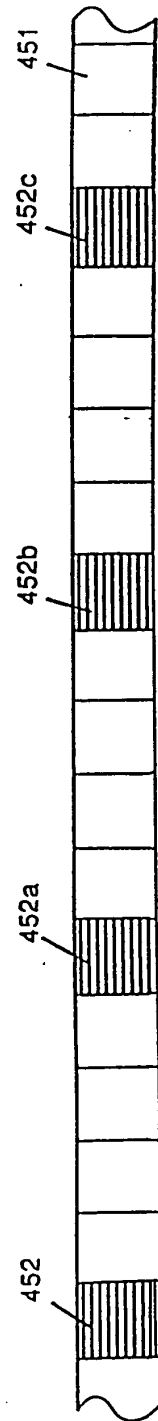
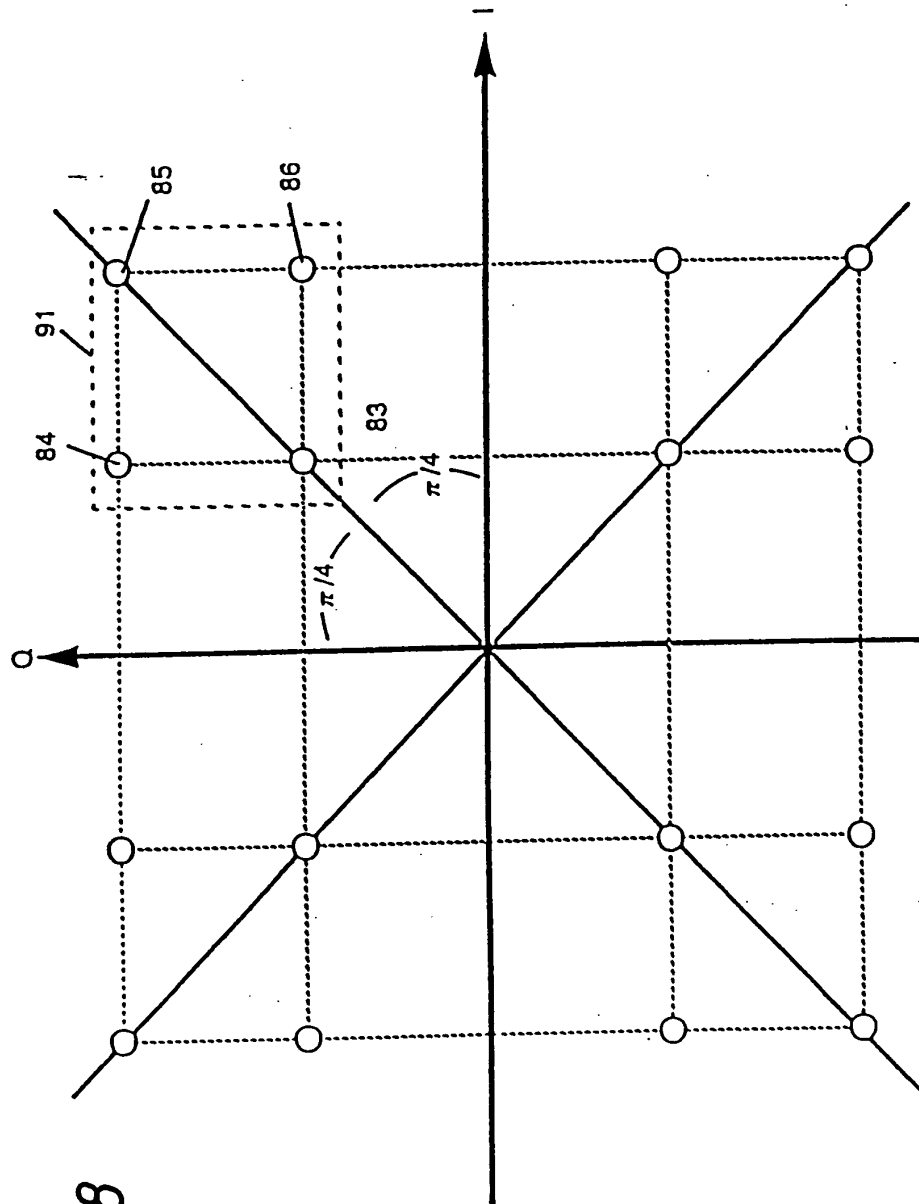


FIG. 38



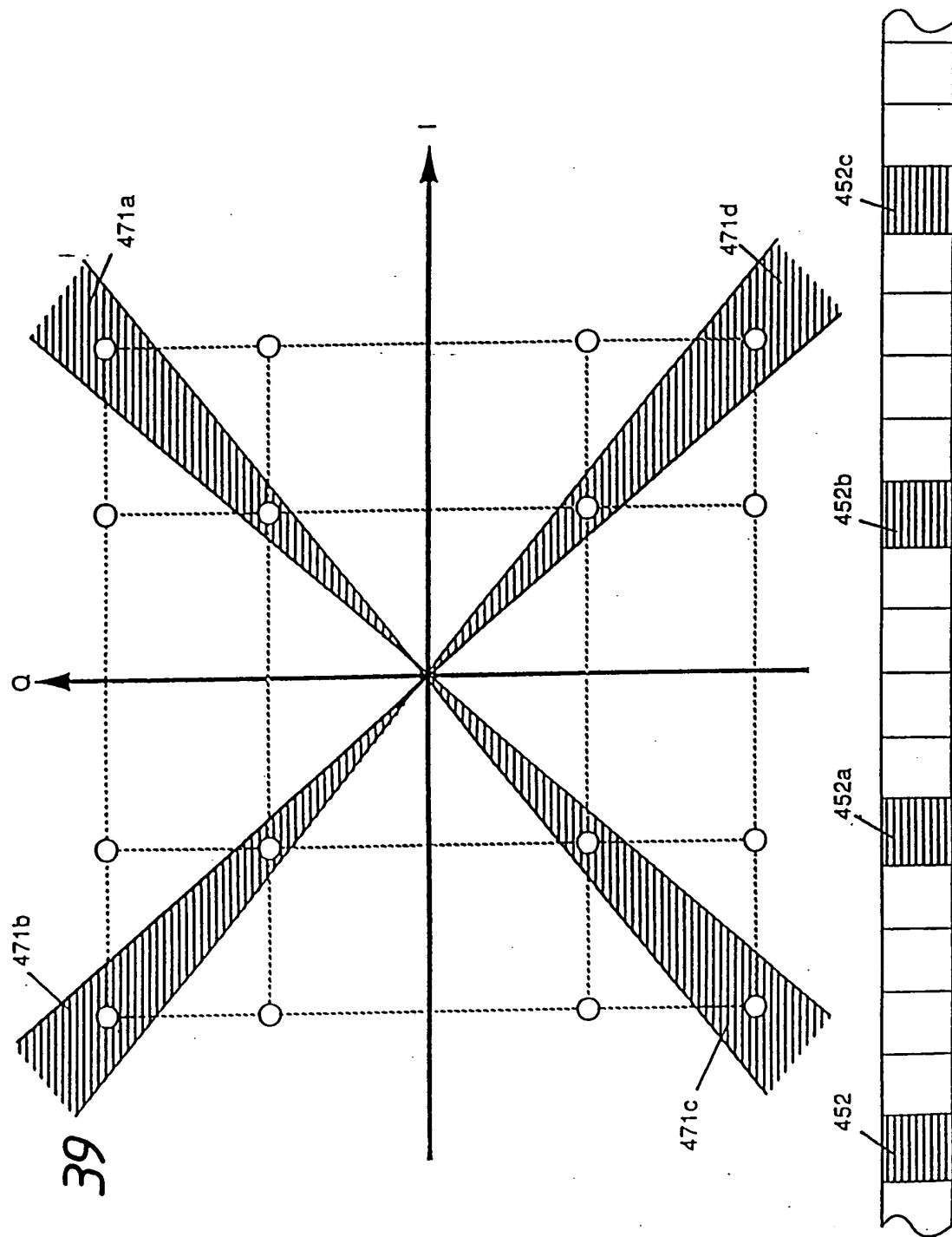


FIG. 40

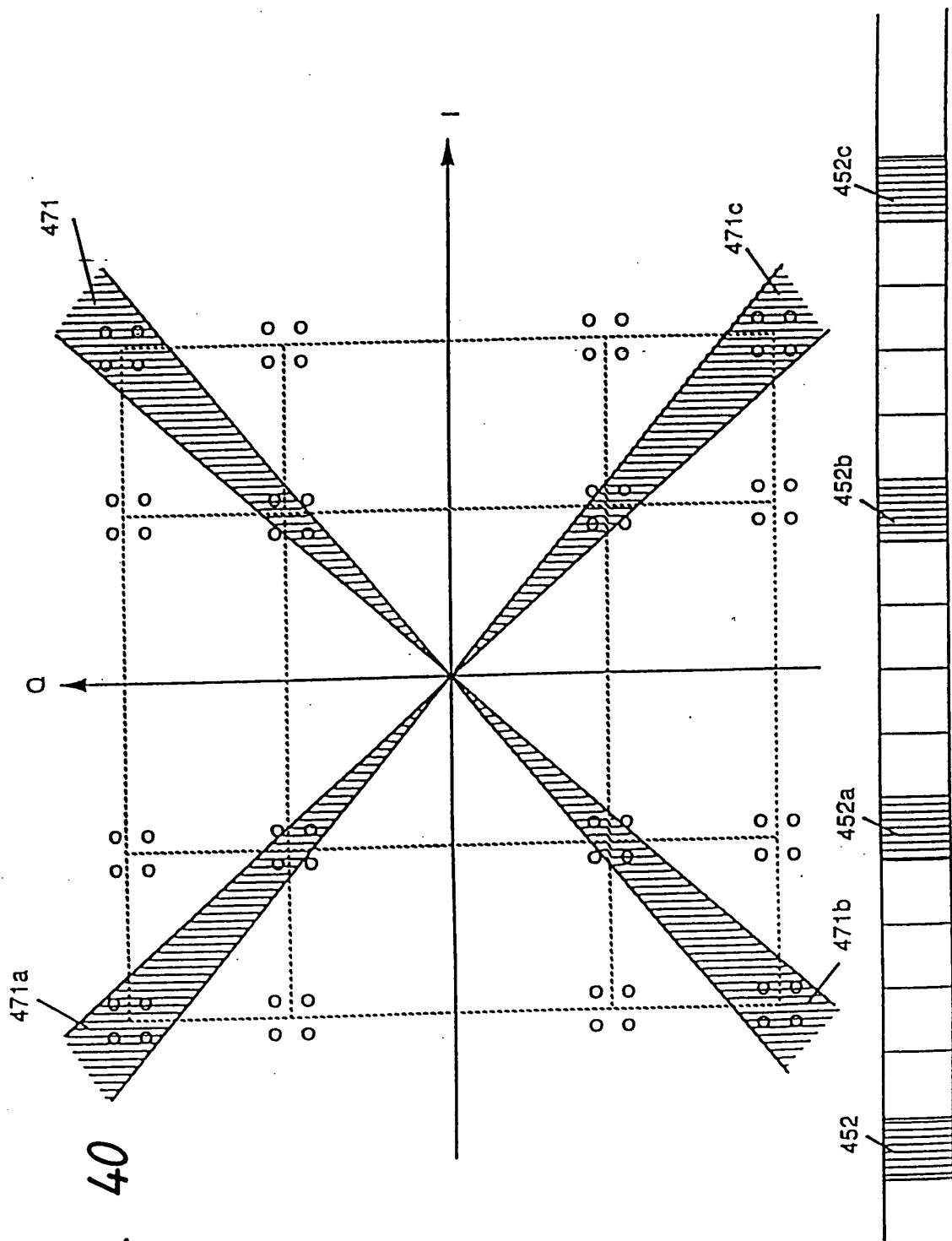


FIG. 41

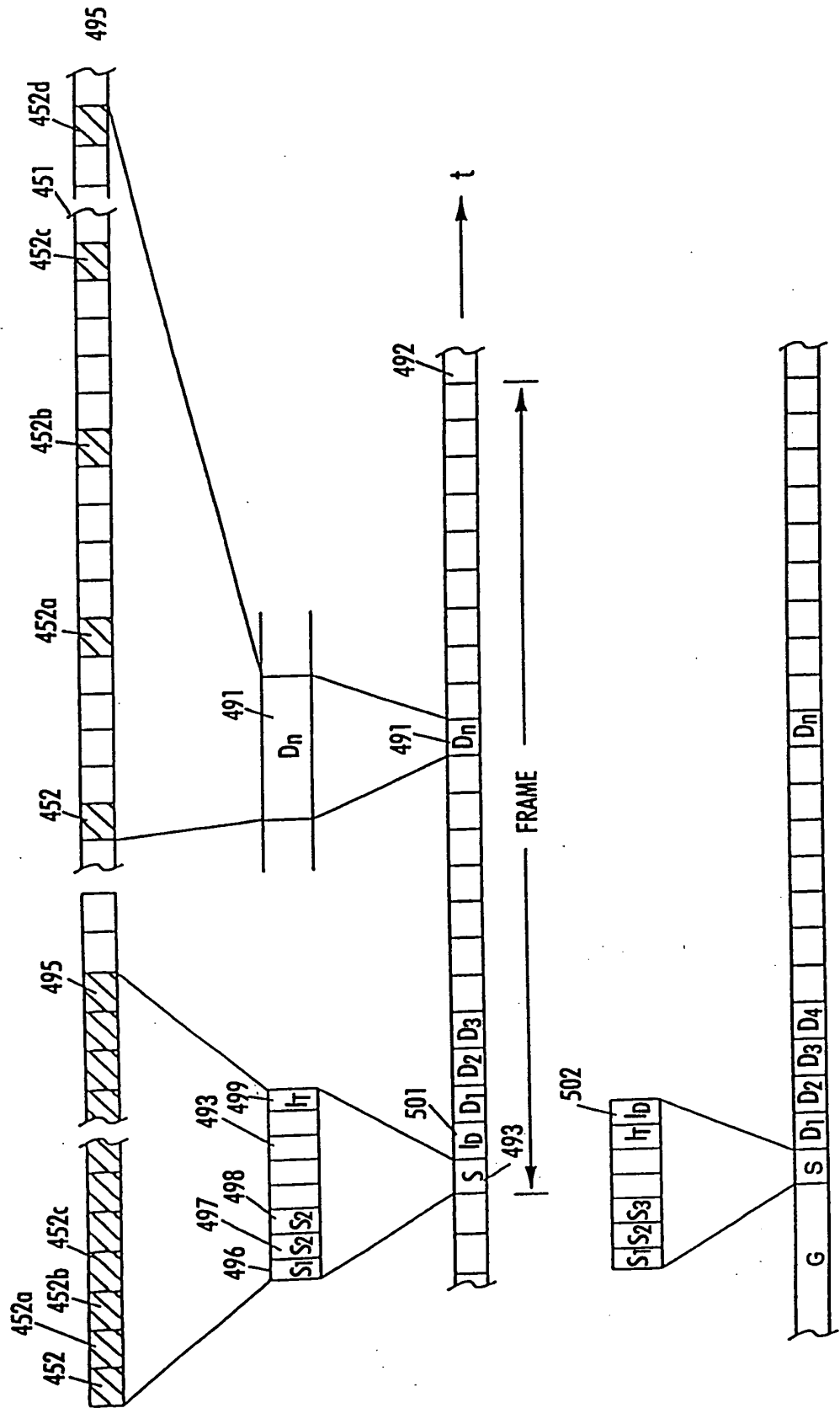


FIG. 42

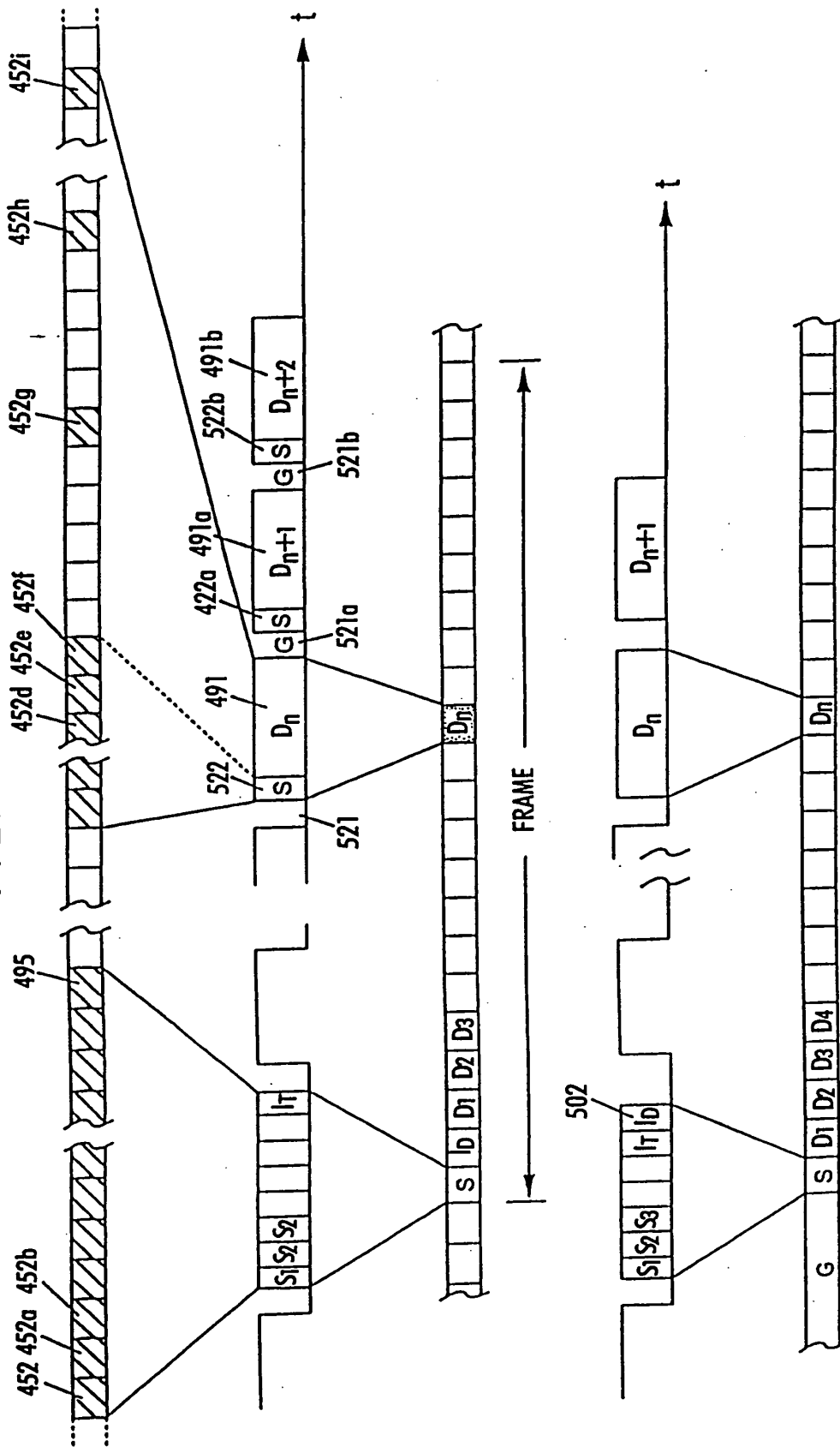


FIG. 43

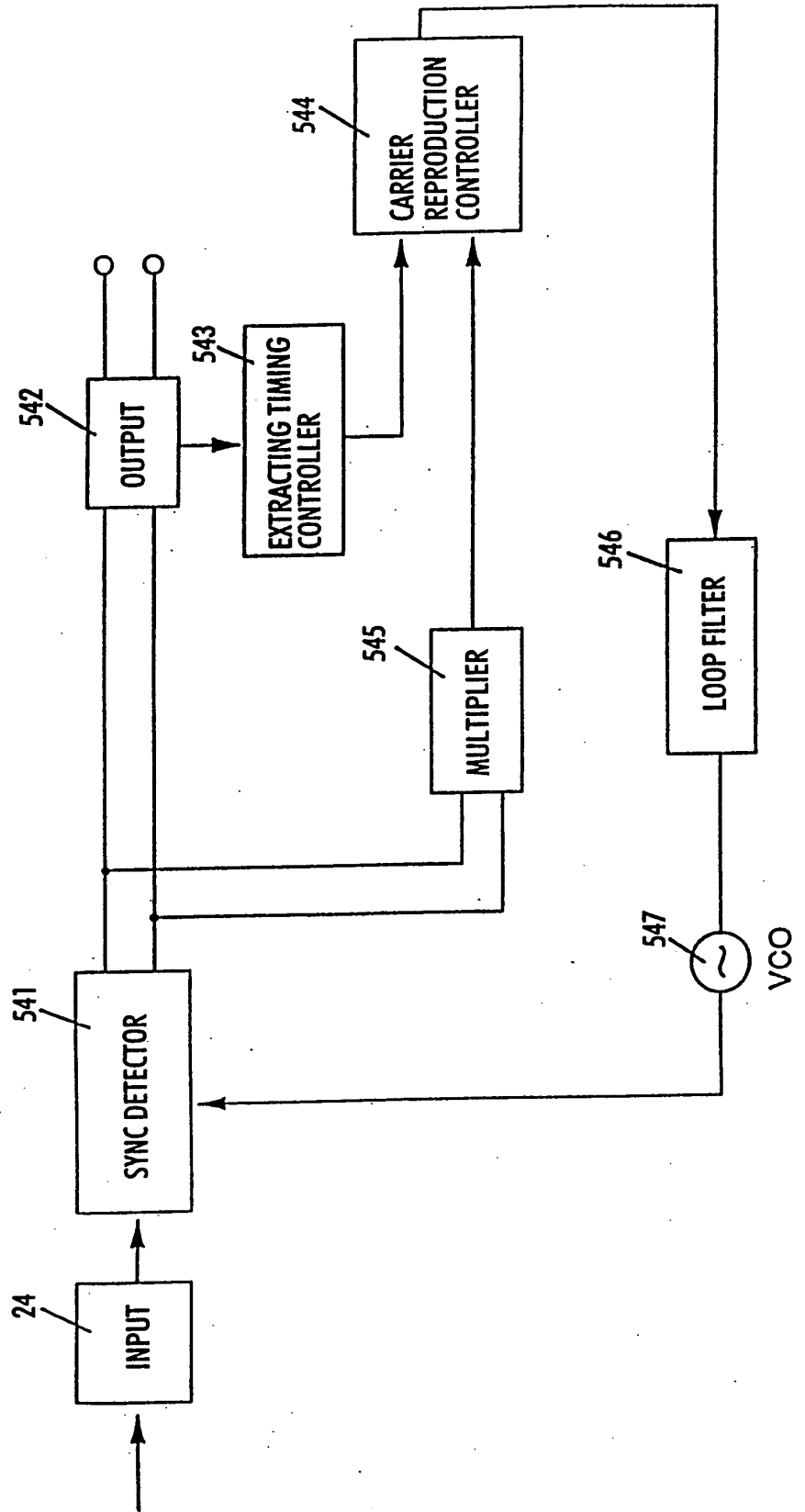


FIG. 44

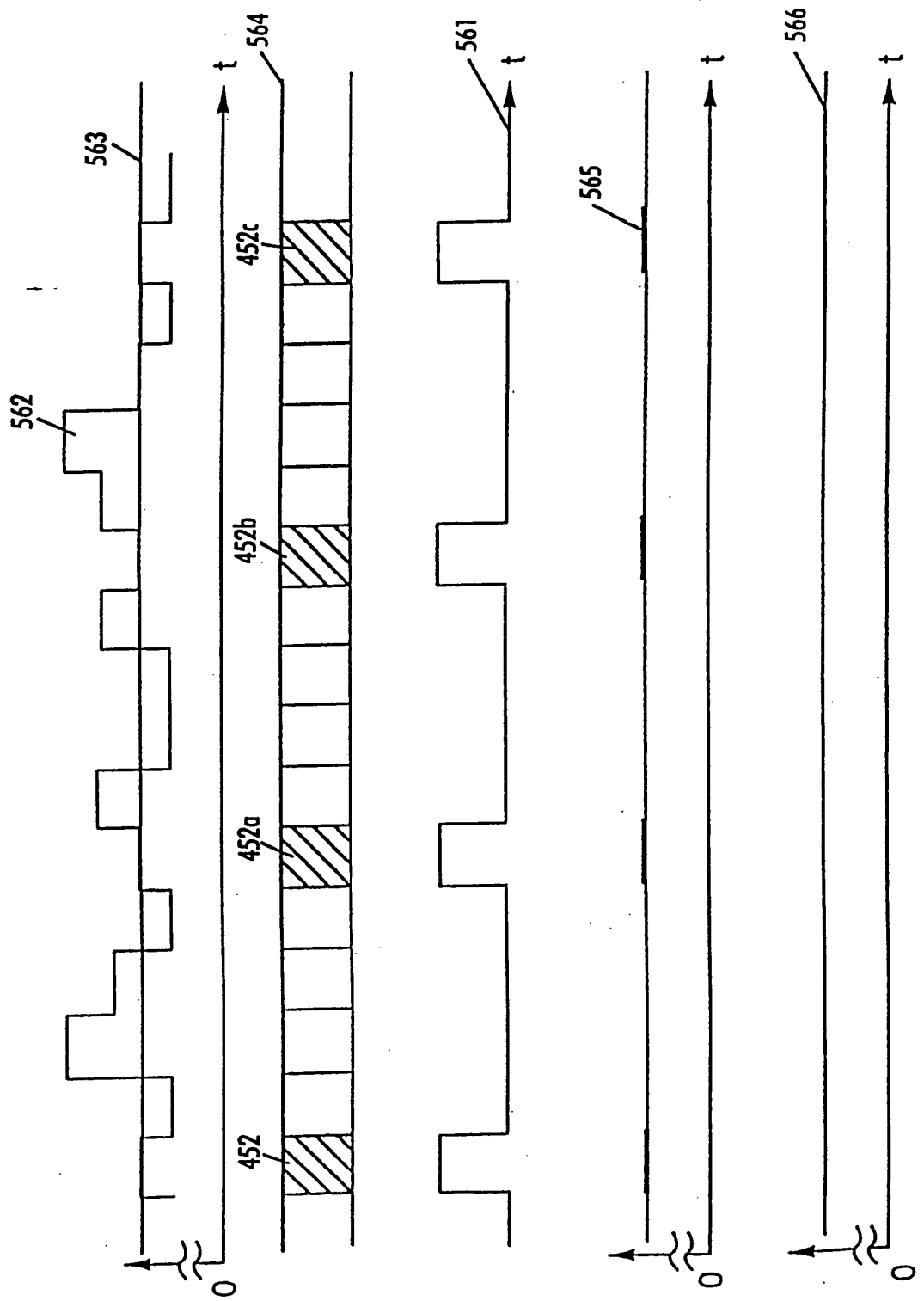


FIG. 45

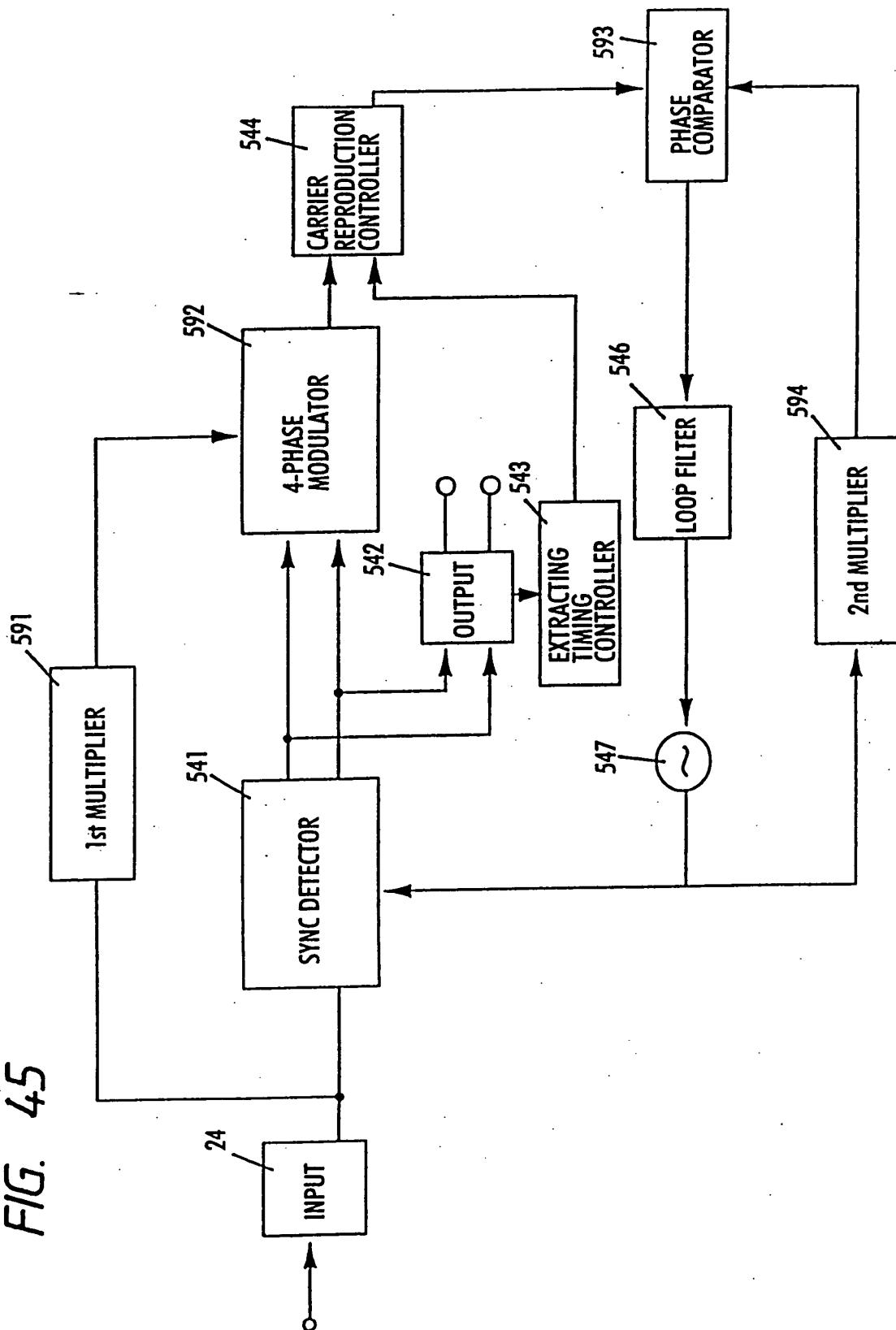


FIG. 46

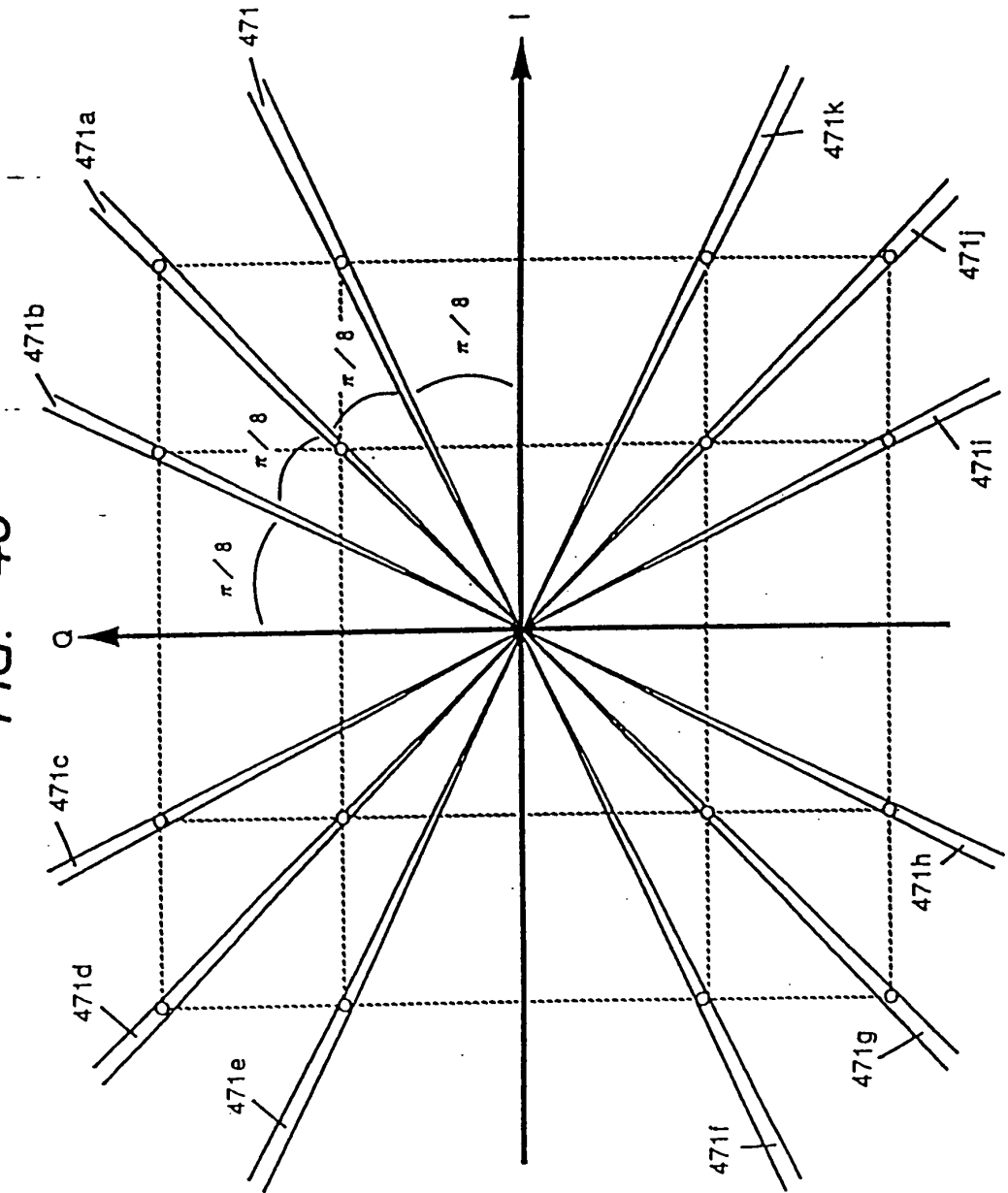
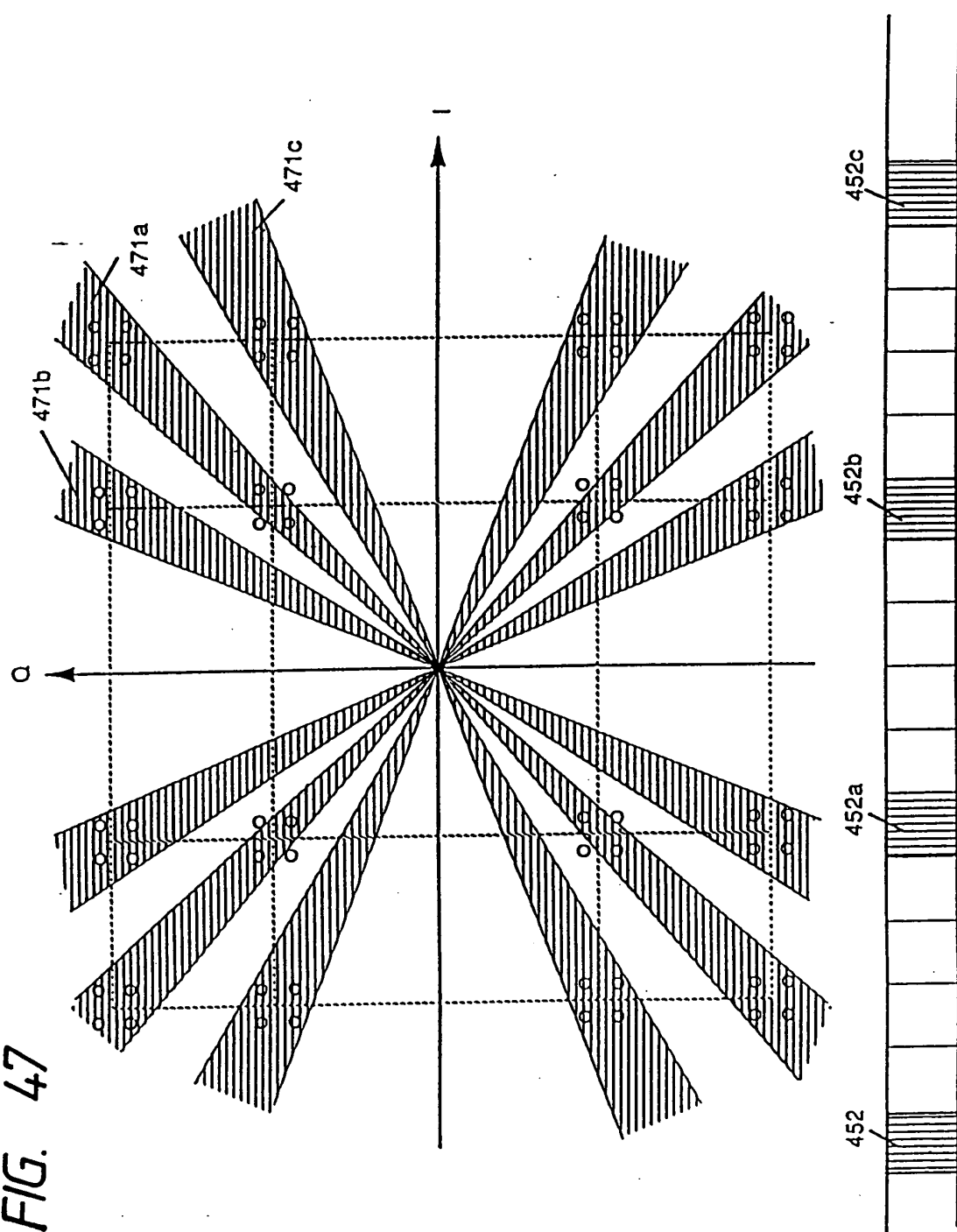


FIG. 47



The diagram illustrates a PLL system with a feedback loop. The input signal enters a **SYNC DETECTOR** (541). The output of the sync detector is fed into the **LOCK DETECTOR** (542) and also branches off to the **LOOP FILTER** (546). The **LOCK DETECTOR** (542) produces two signals, $\sin \theta$ and $\cos \theta$. These signals are fed into a series of multipliers and adders/subtractors. The first stage consists of multipliers 665 and 664, followed by an **ADDER** (662) and a **SUBTRACTOR** (663). The outputs of this stage are fed into a second stage of multipliers 666 and 667, followed by an **ADDER** (667) and a **SUBTRACTOR** (668). The outputs of the second stage are fed into a third stage of multipliers 670 and 674, followed by an **ADDER** (671) and a **SUBTRACTOR** (672). The output of the third stage is fed into the **LOOP FILTER** (546). The output of the loop filter is fed back to the **LOCK DETECTOR** (541) and also branches off to the **LOCK DETECTOR** (542). The output of the lock detector is fed into the **OUTPUT** (542).

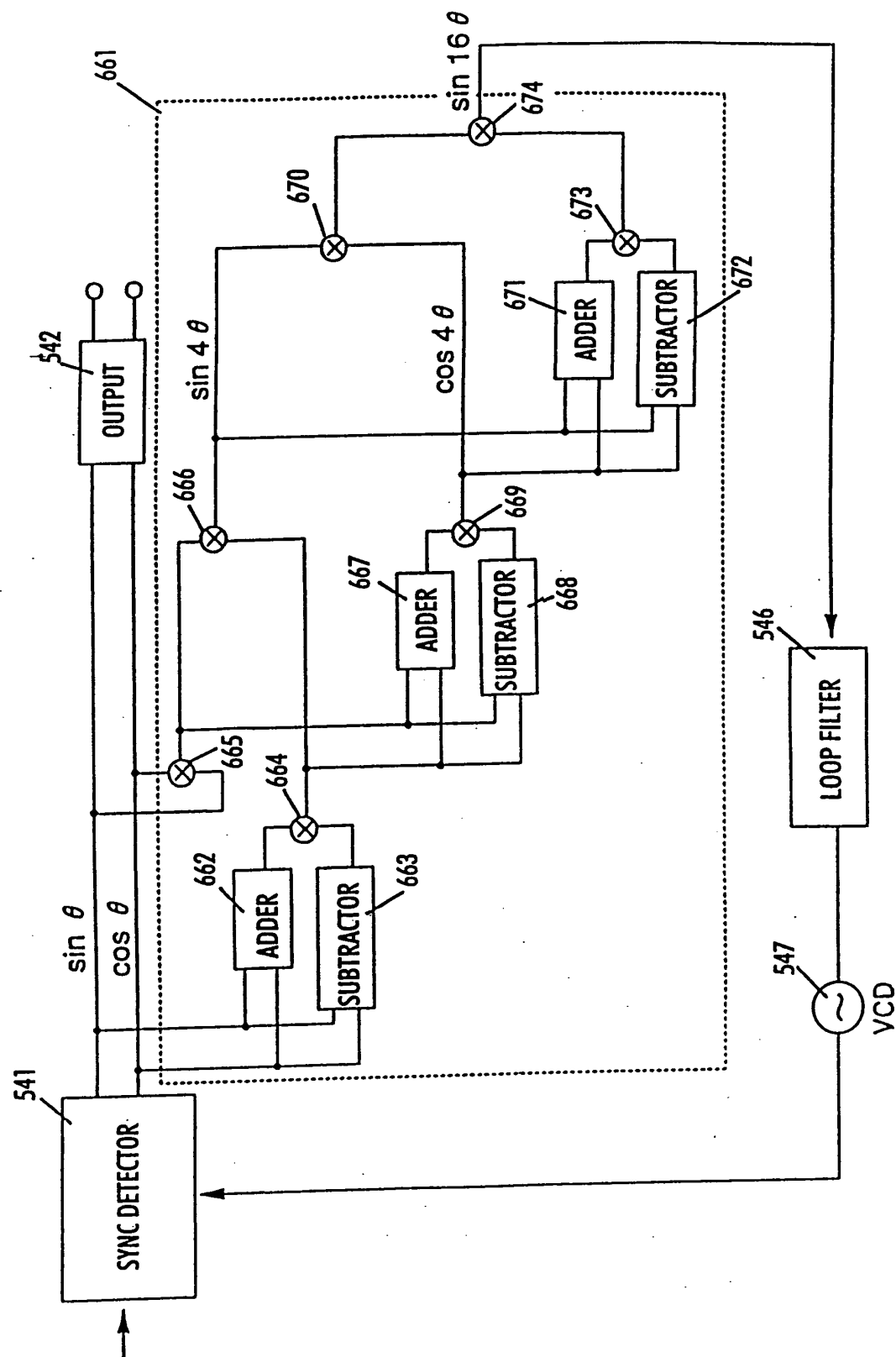


FIG. 49

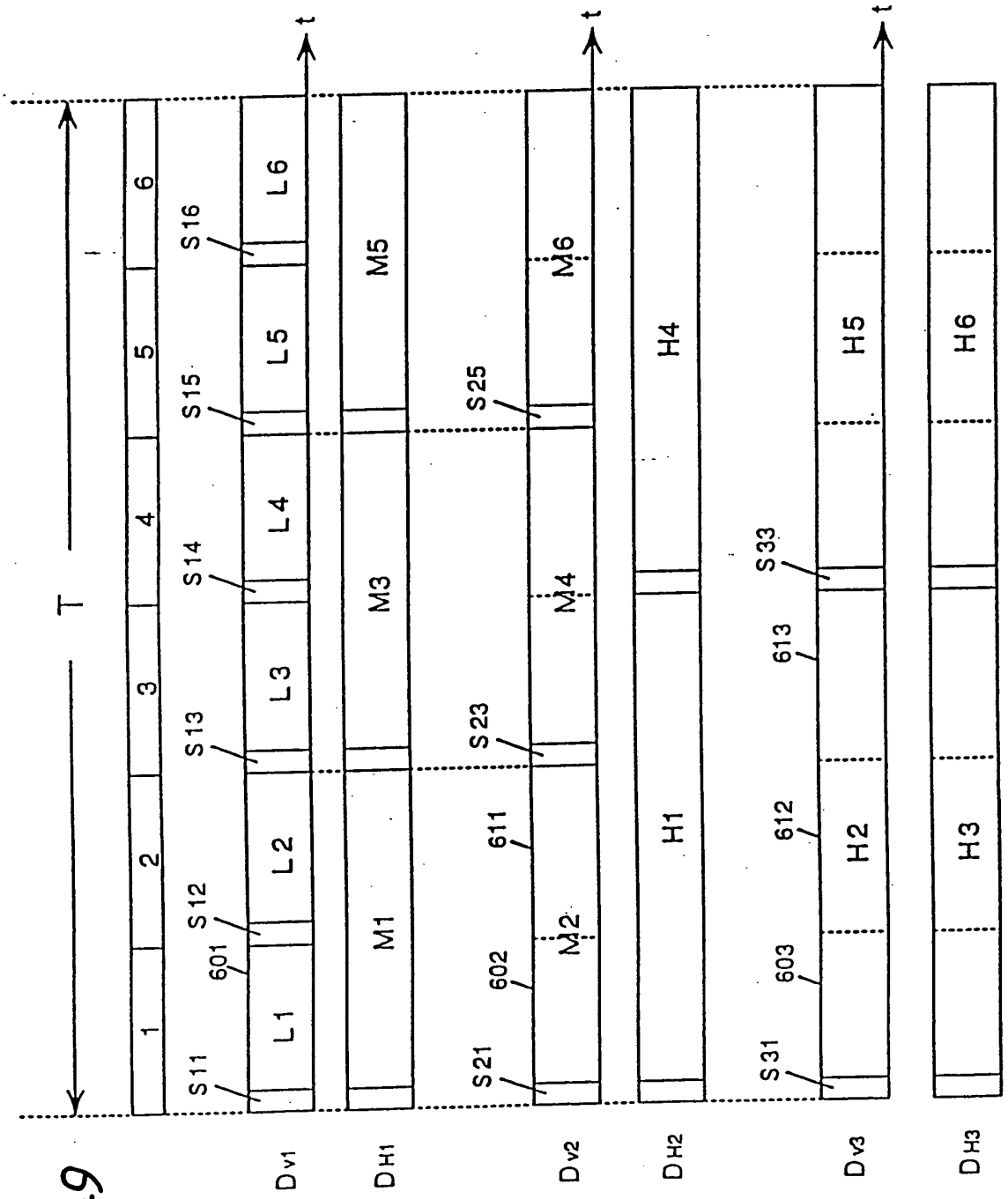


FIG. 50

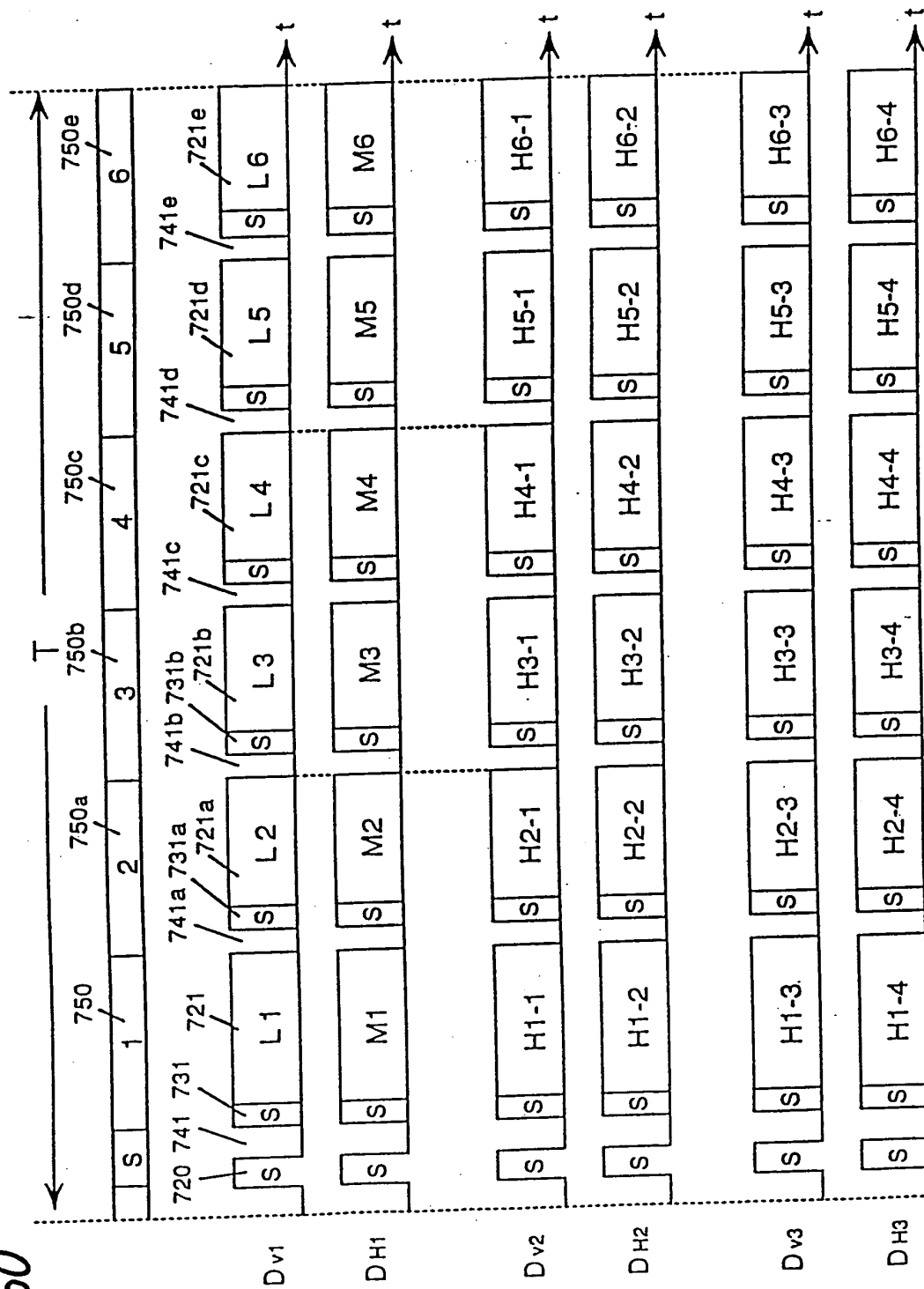


FIG. 51

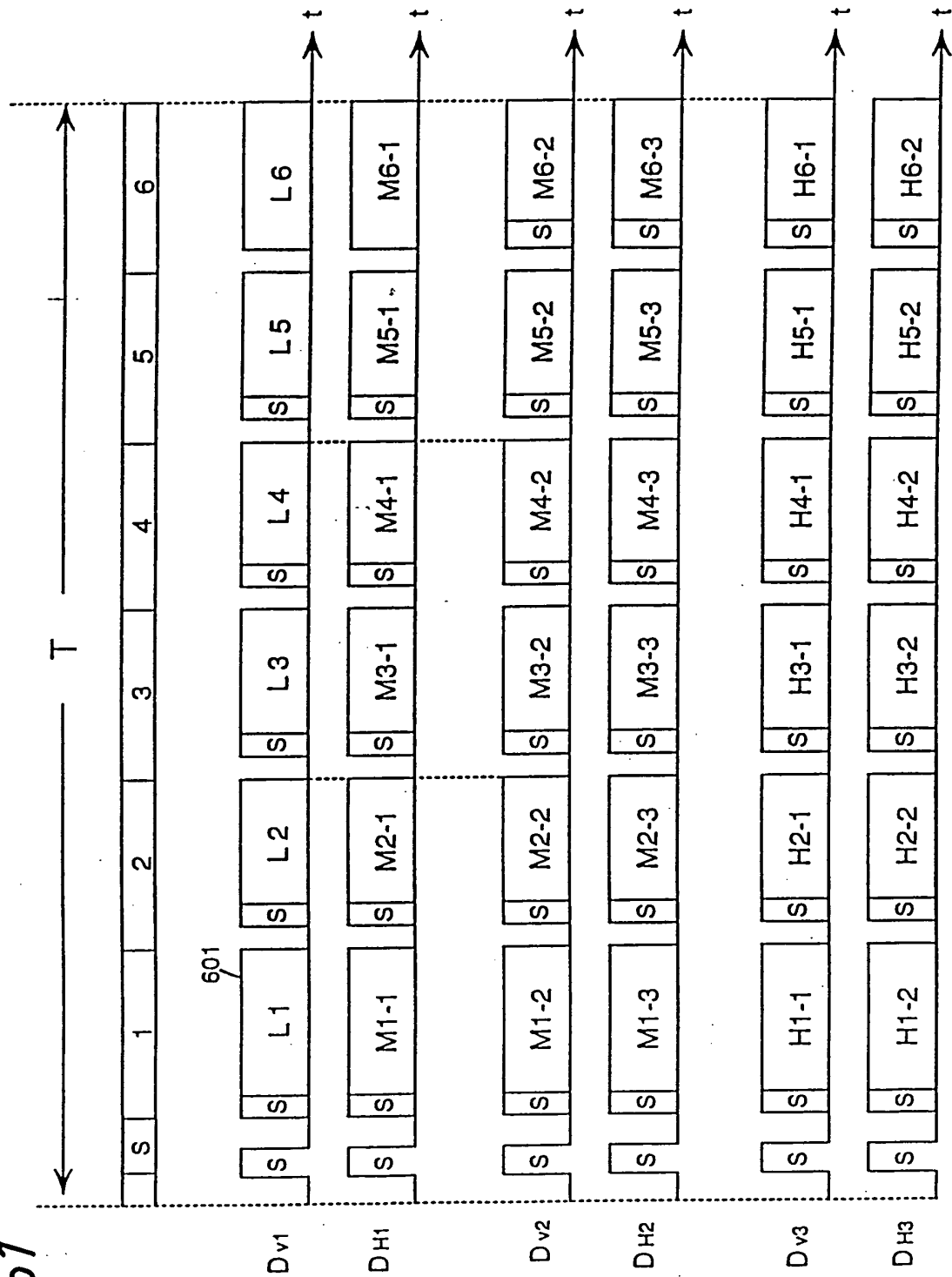


FIG. 52

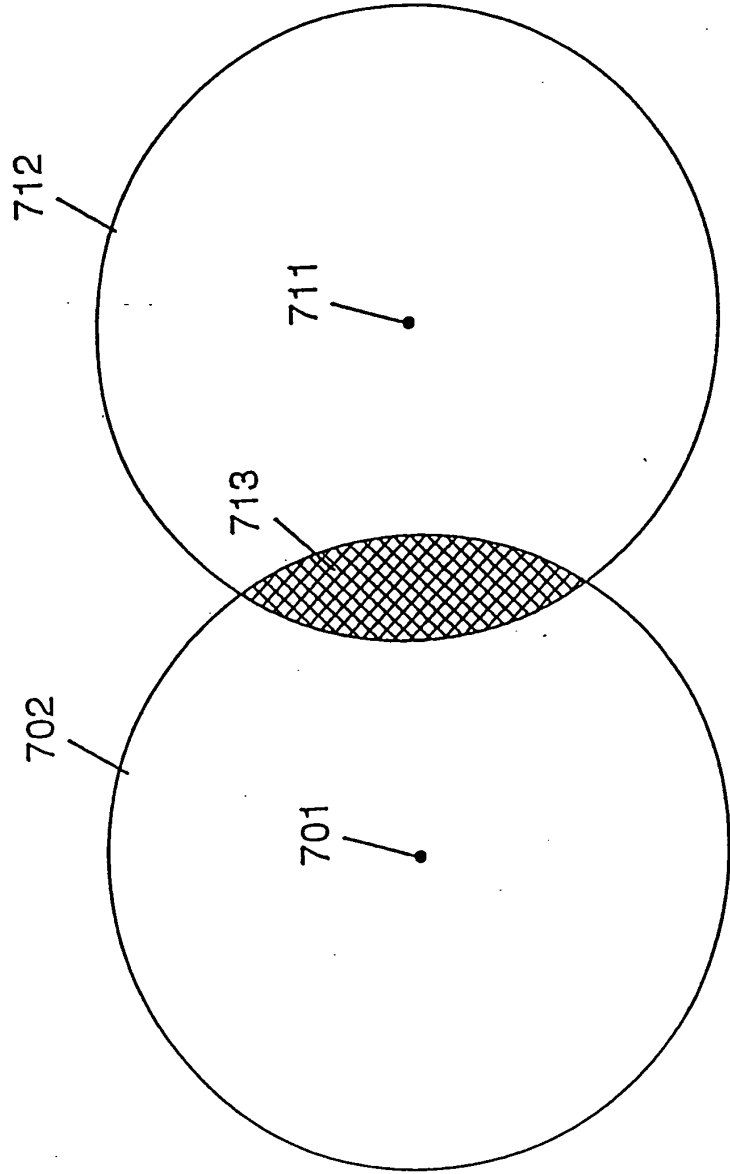


FIG. 53

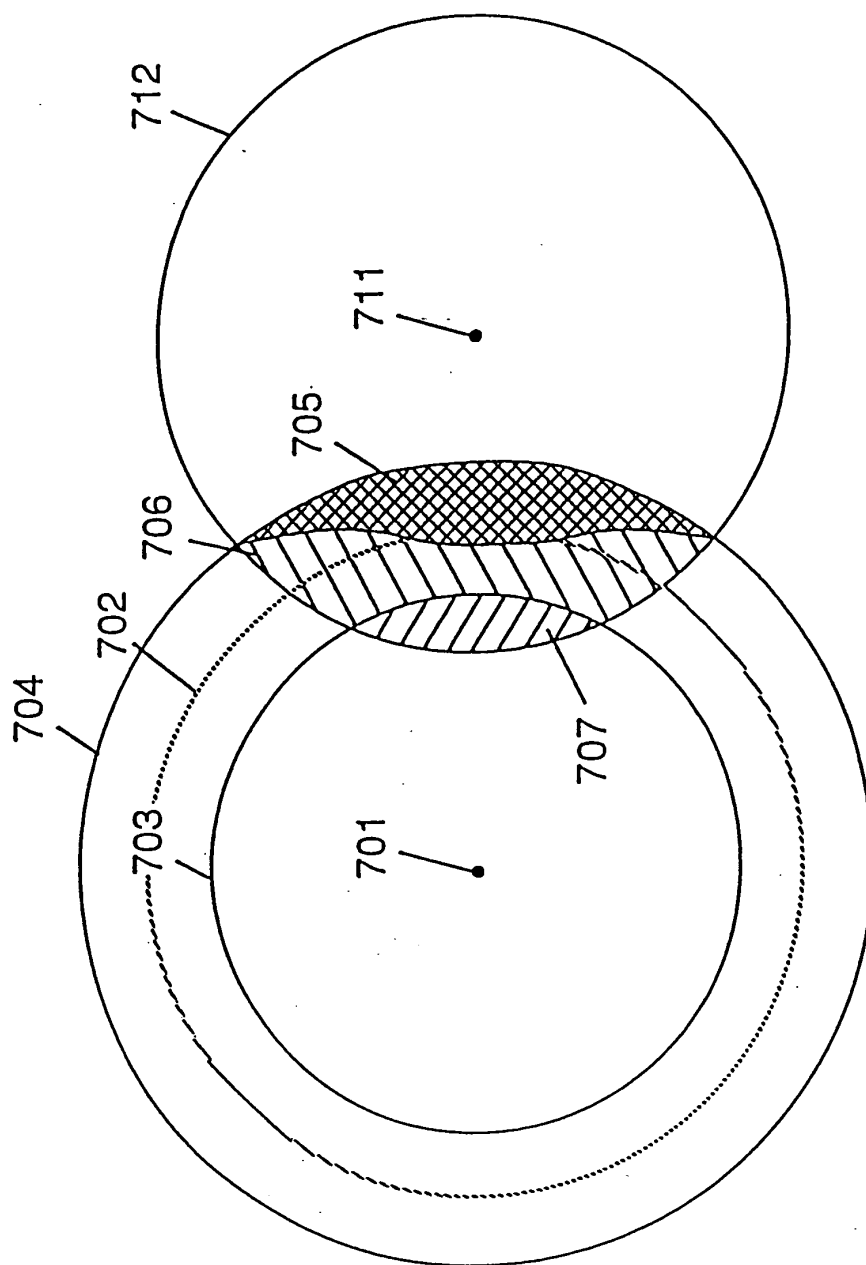


FIG. 54

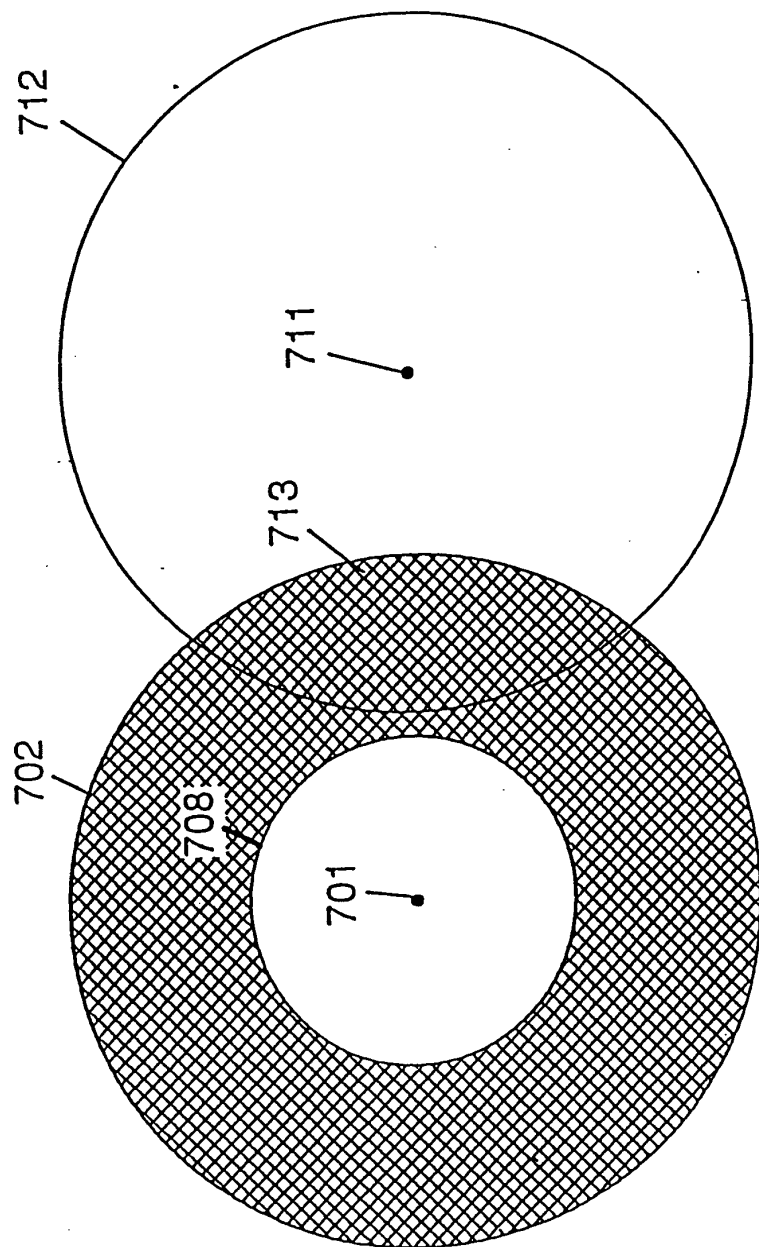


FIG. 55

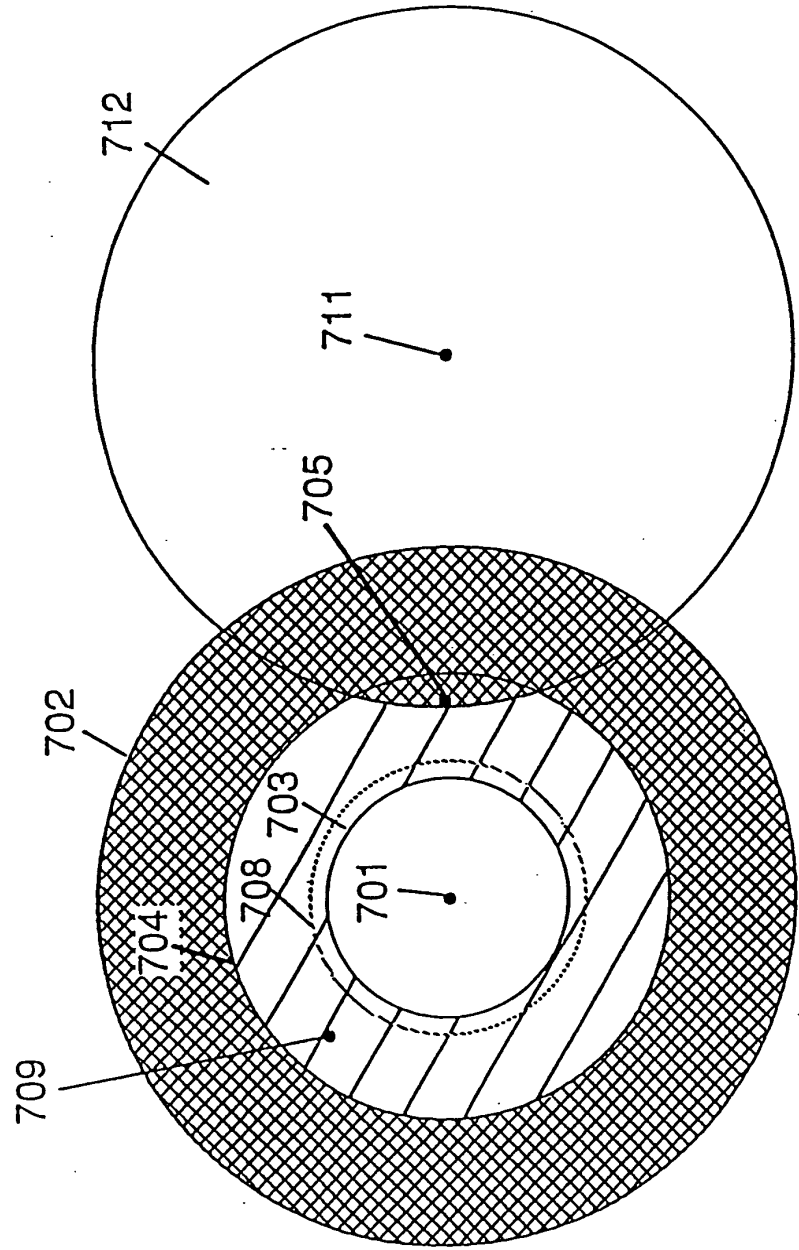


FIG. 56

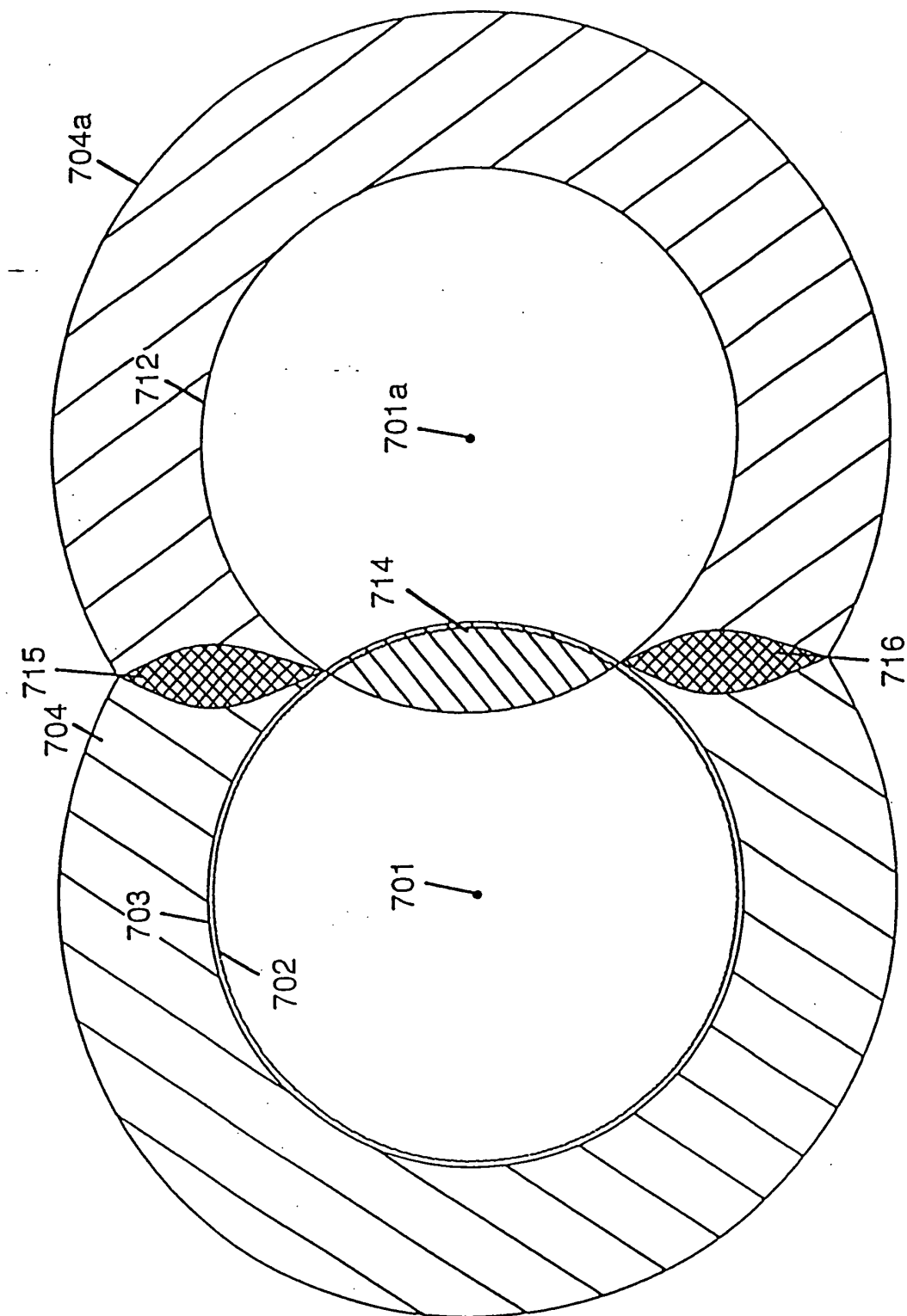


FIG. 57

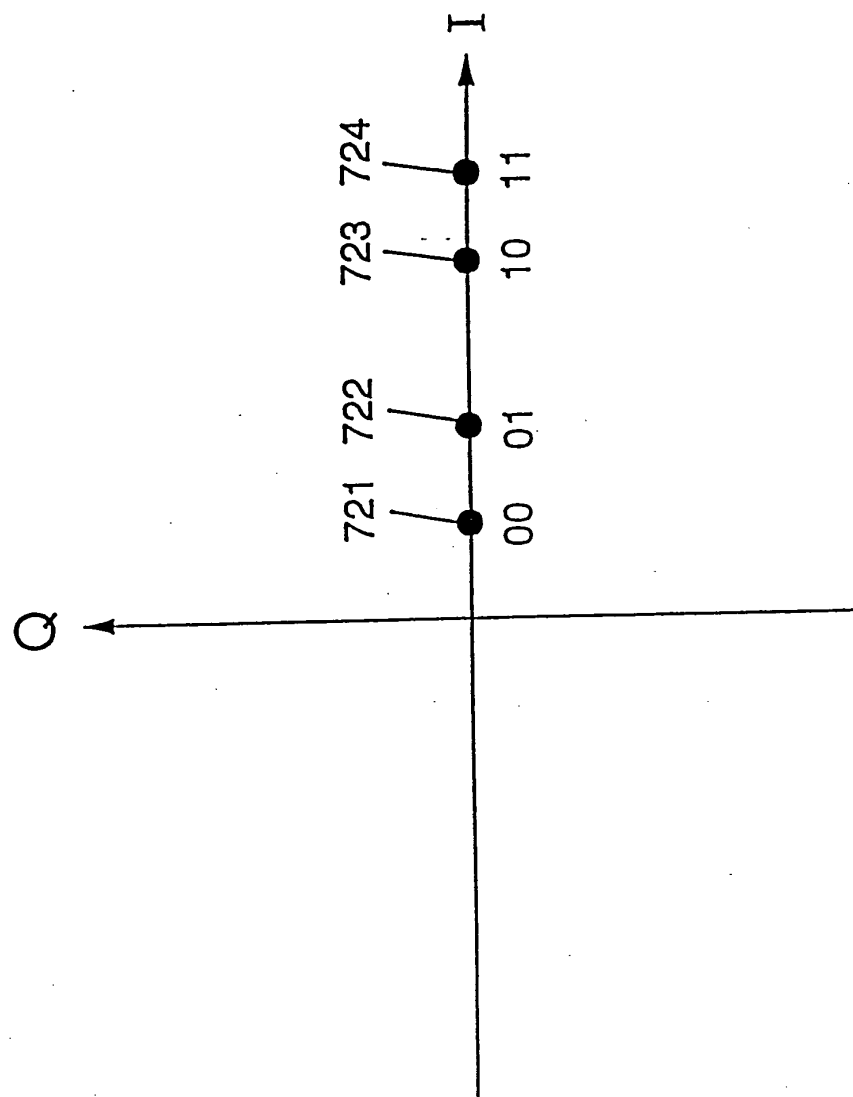
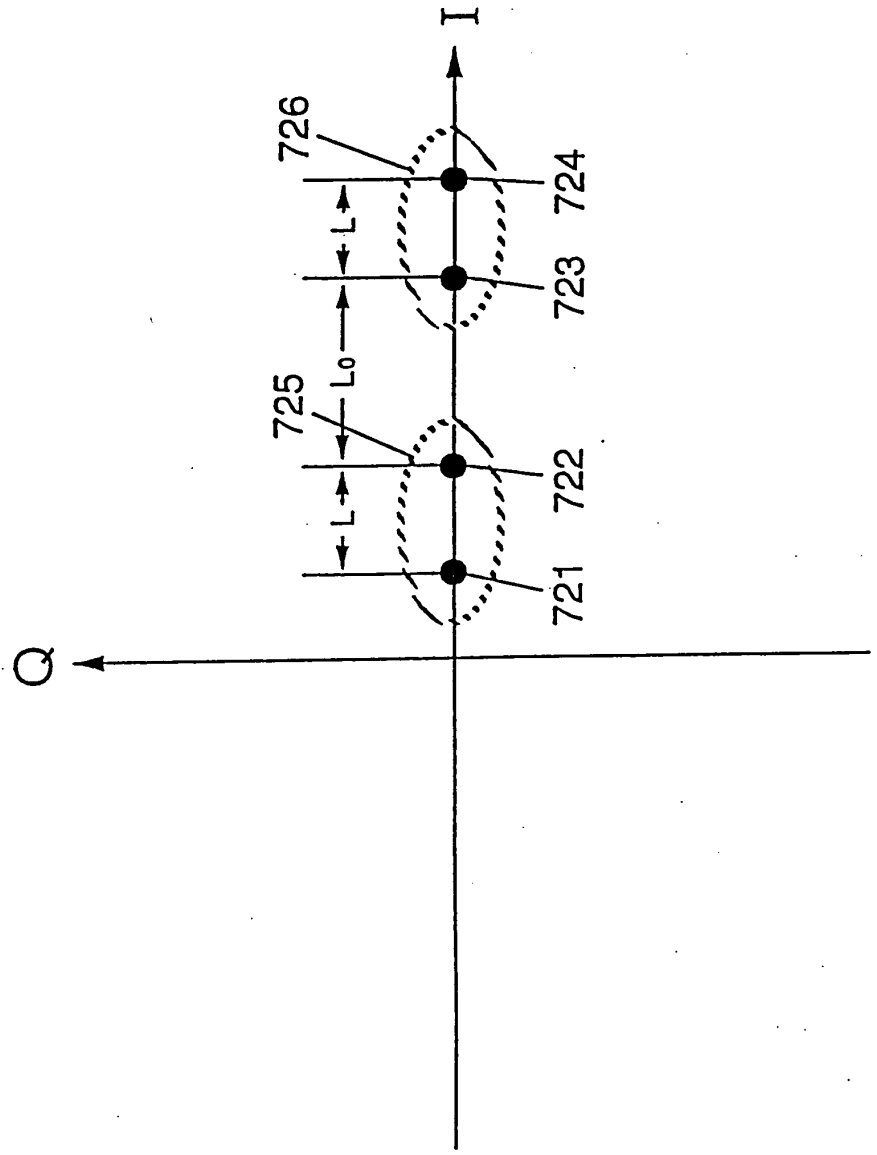


FIG. 58



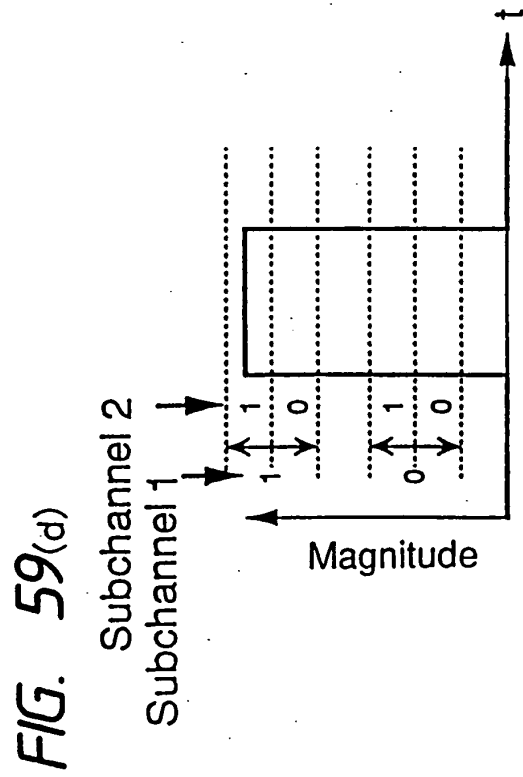
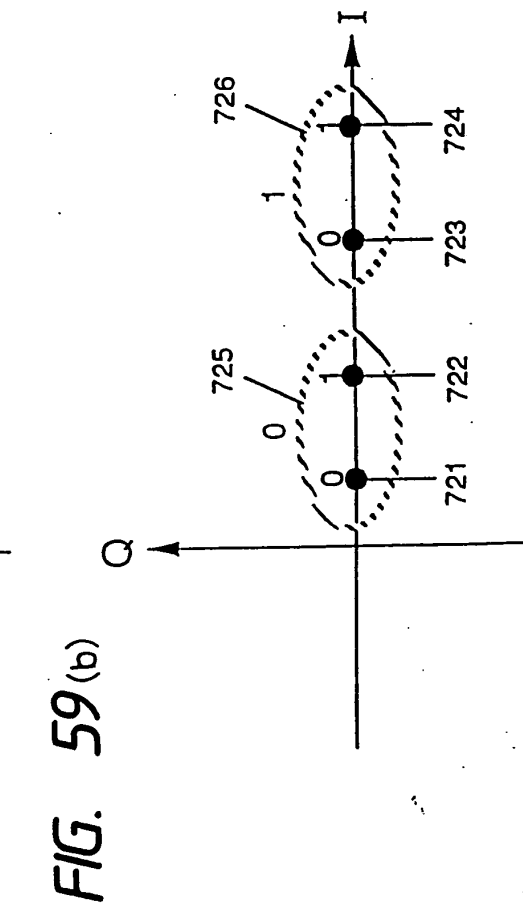
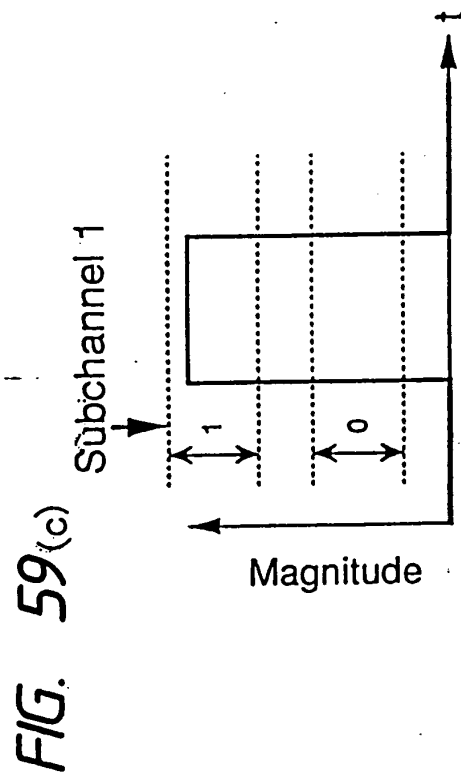
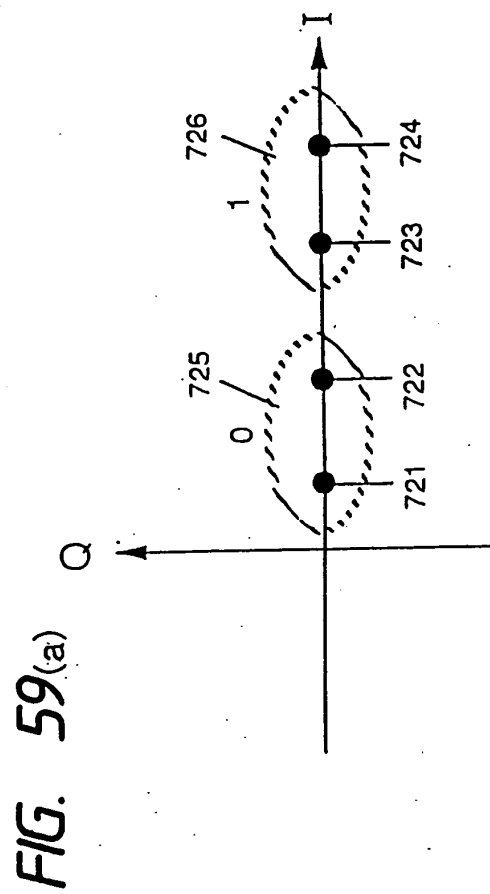


FIG. 60

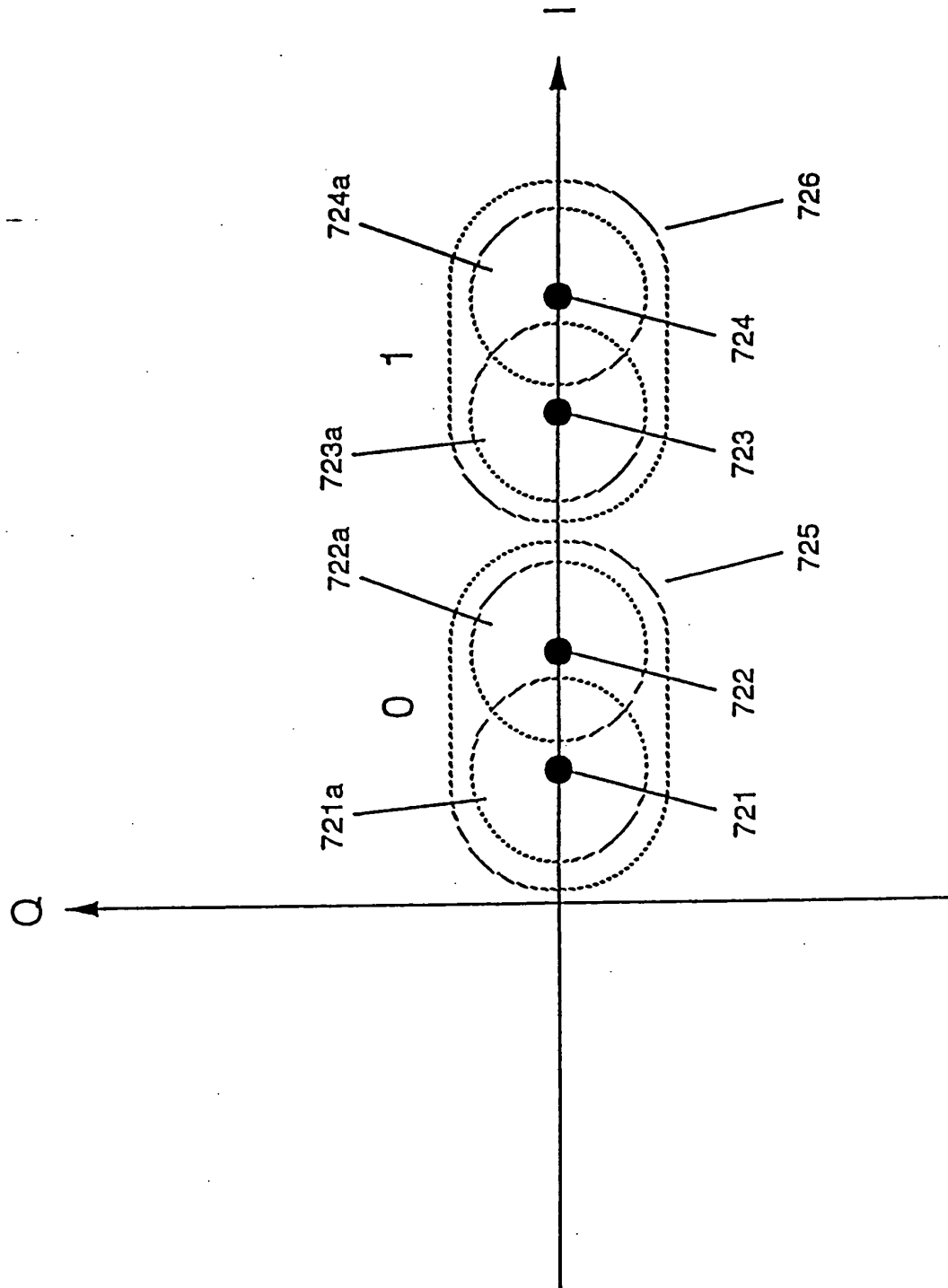


FIG. 61

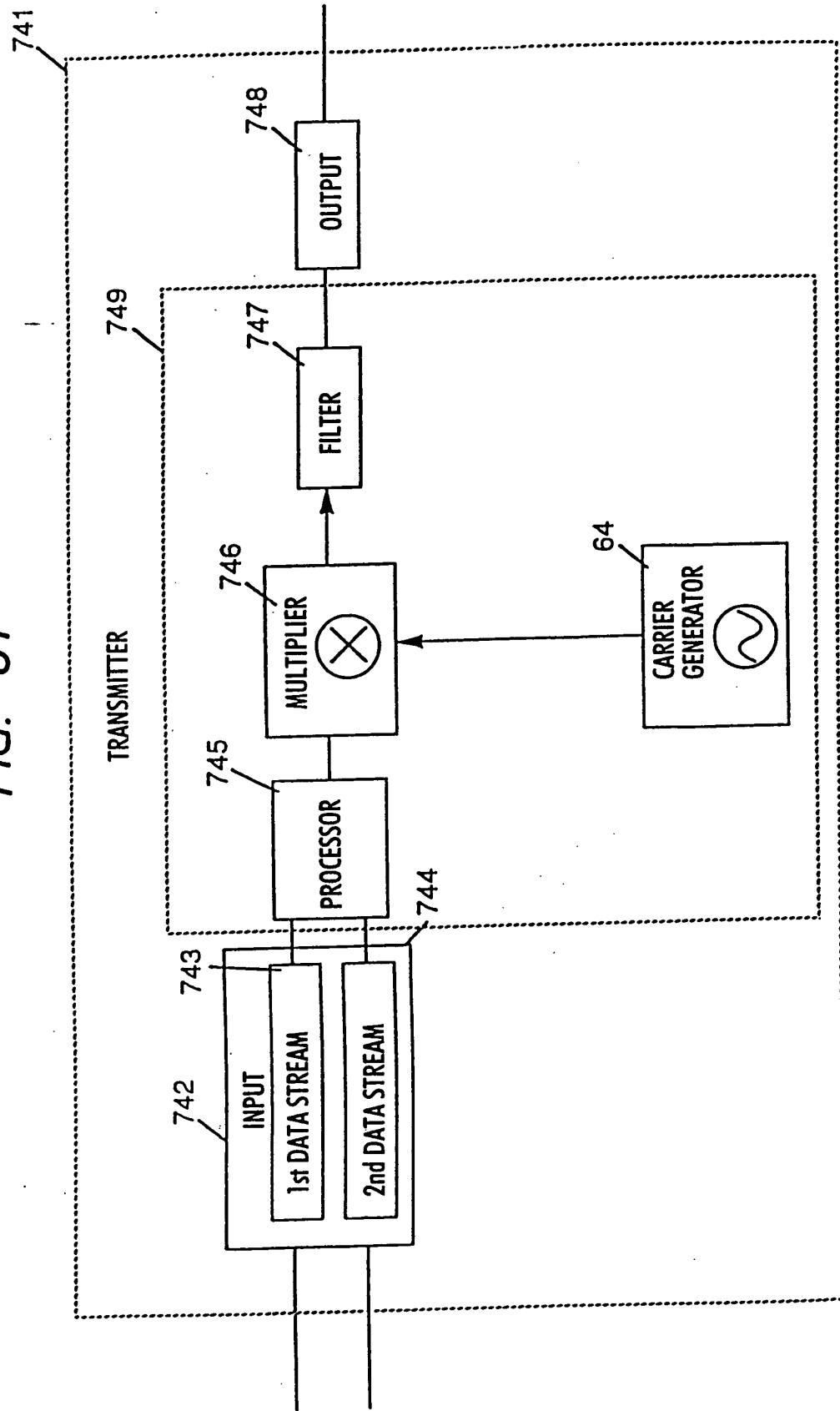


FIG. 62 (a)

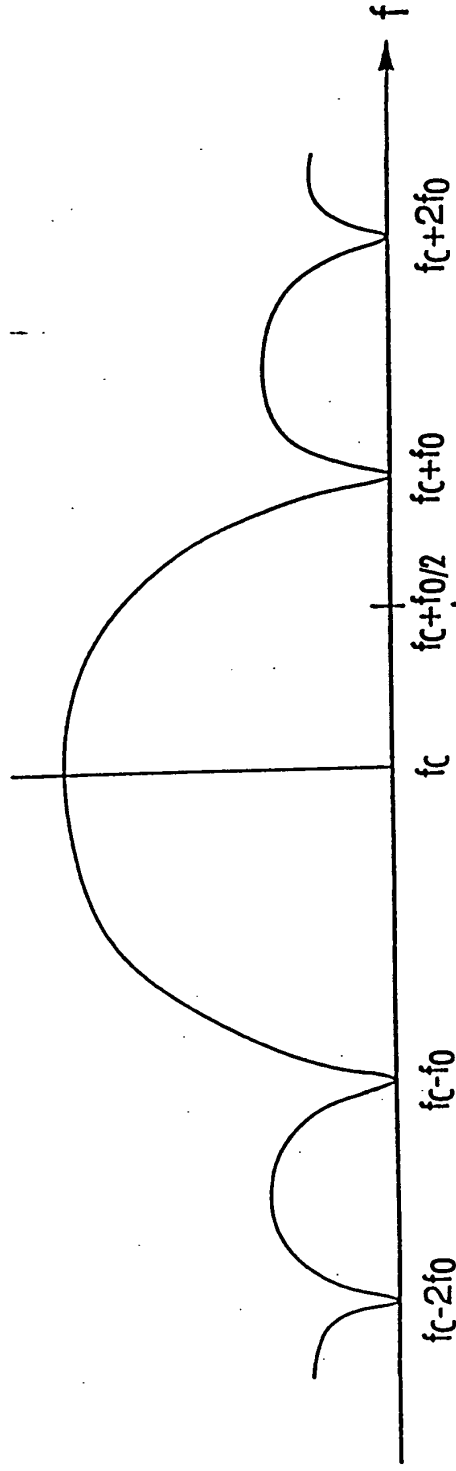


FIG. 62 (b)

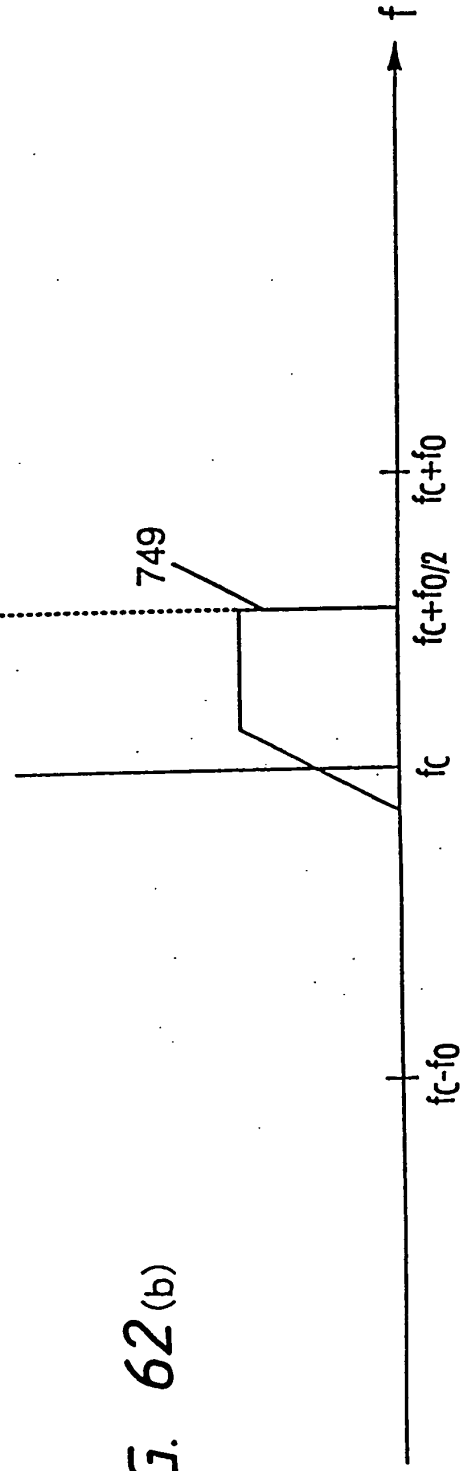


FIG. 63

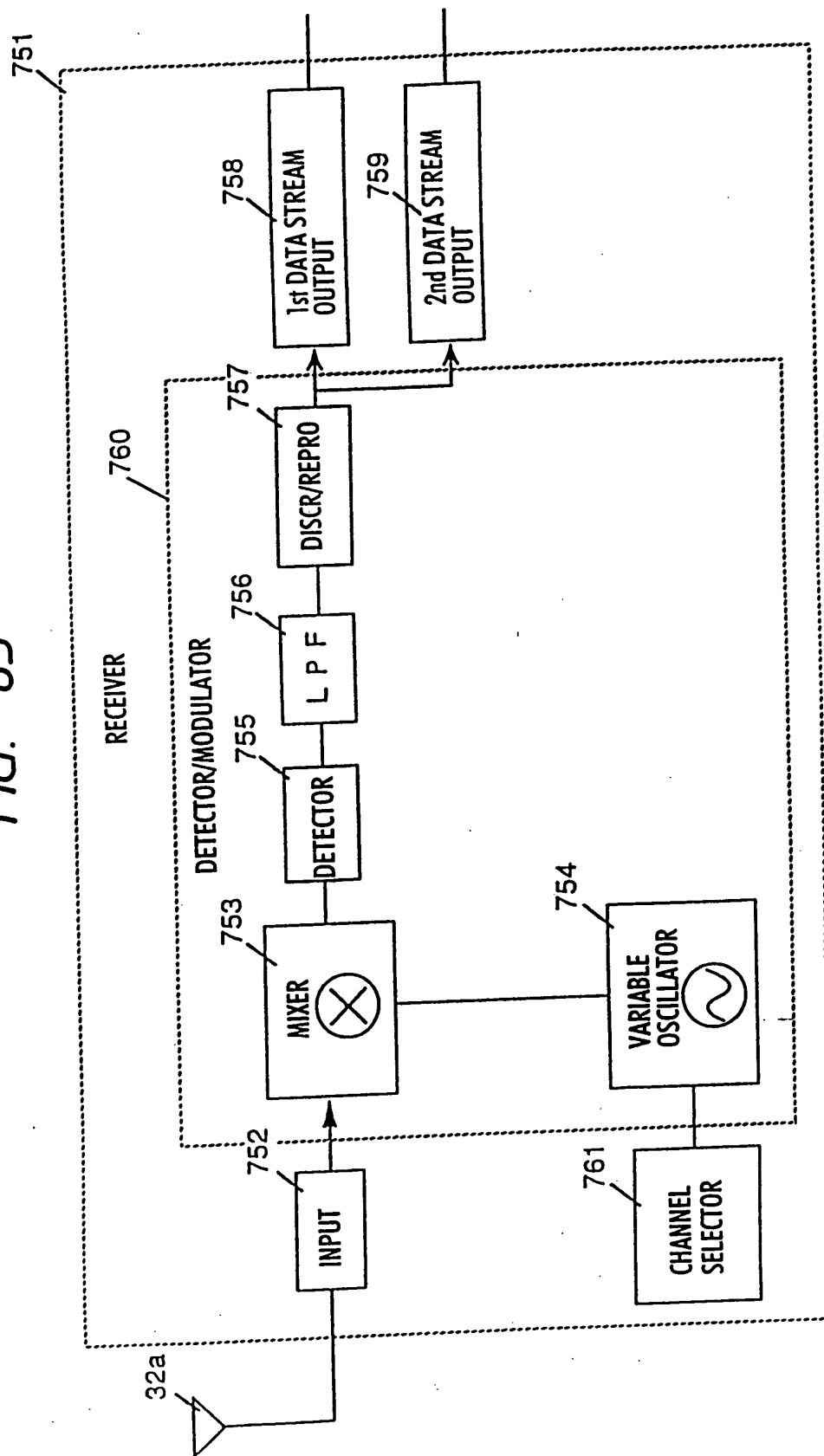


FIG. 64

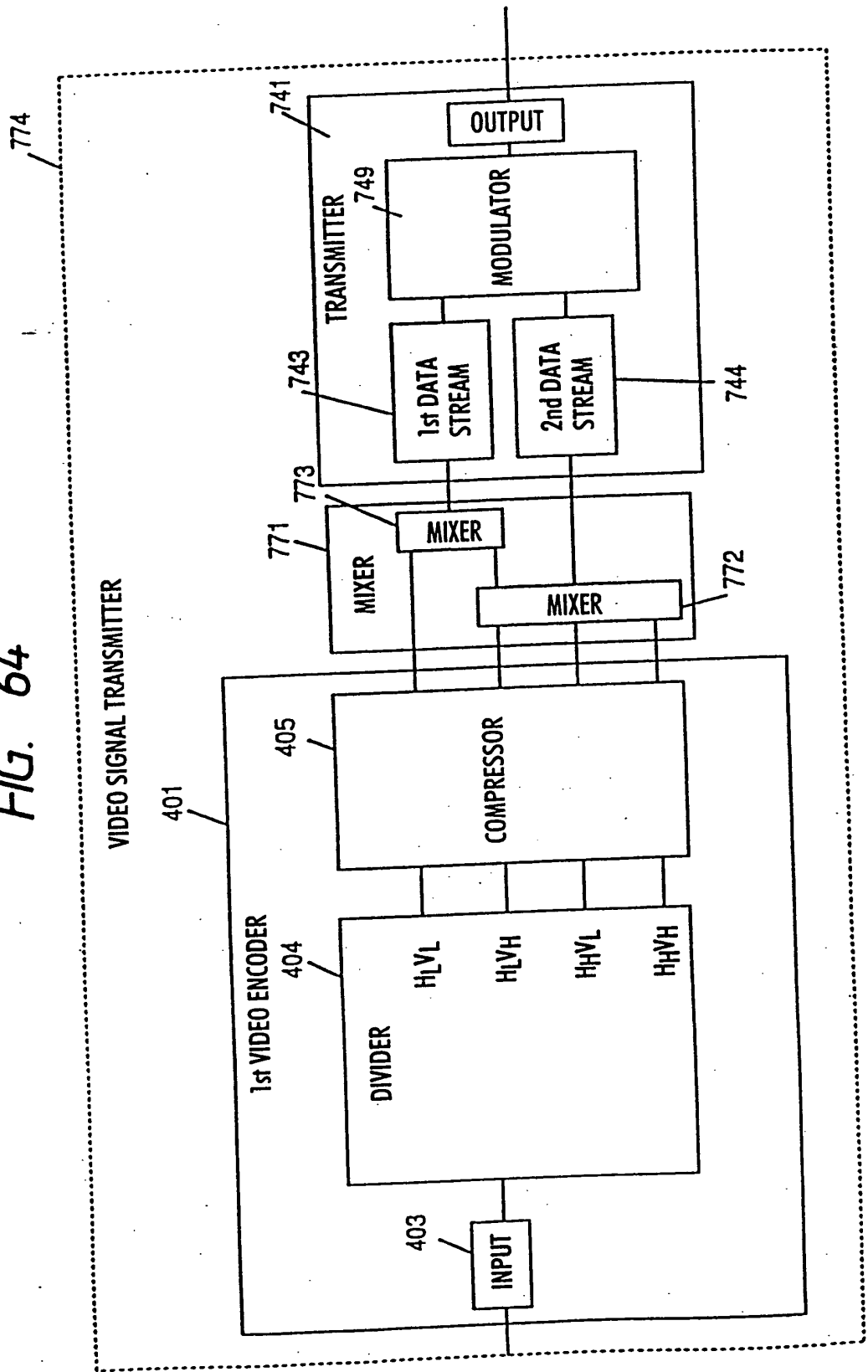


FIG. 65

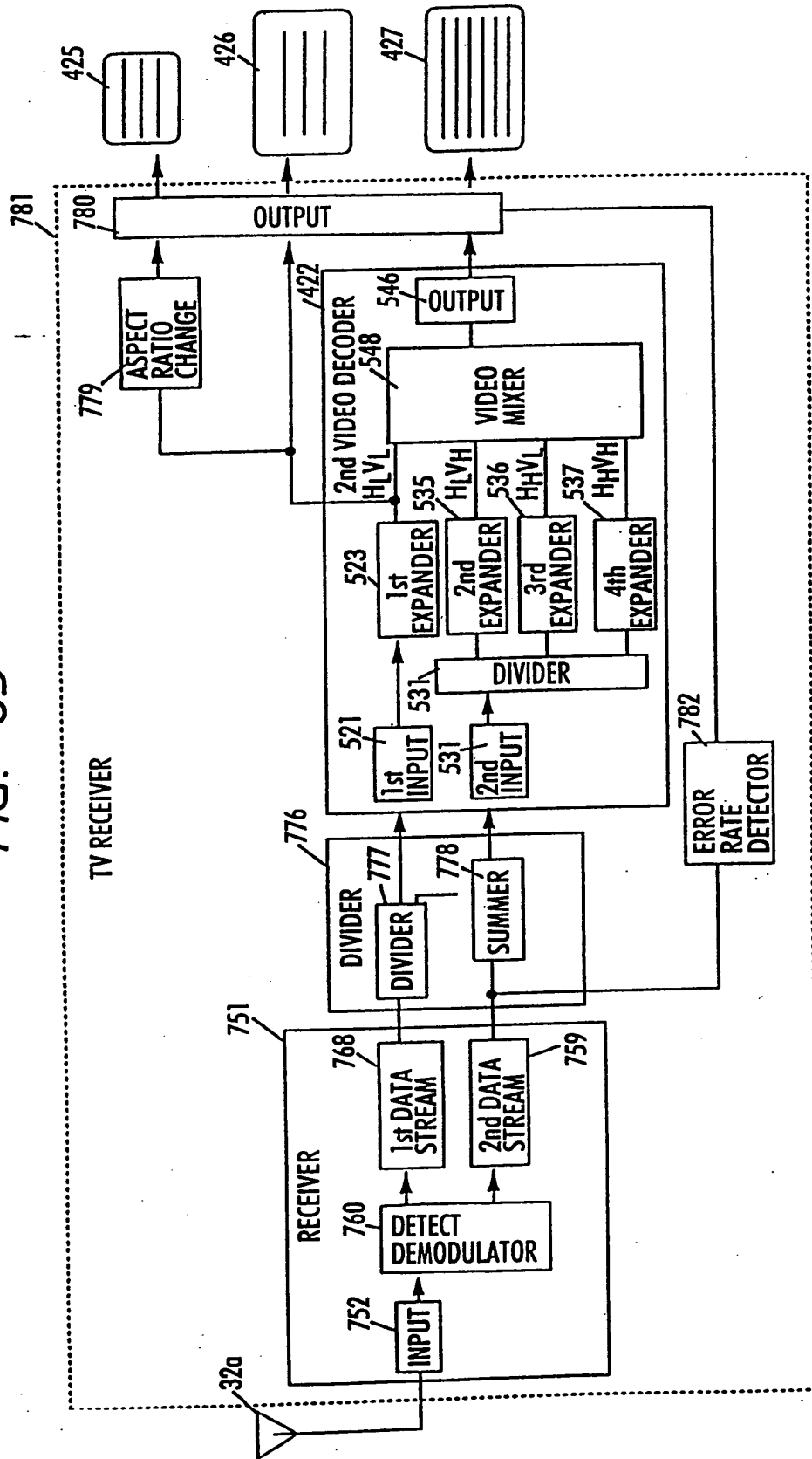


FIG. 66

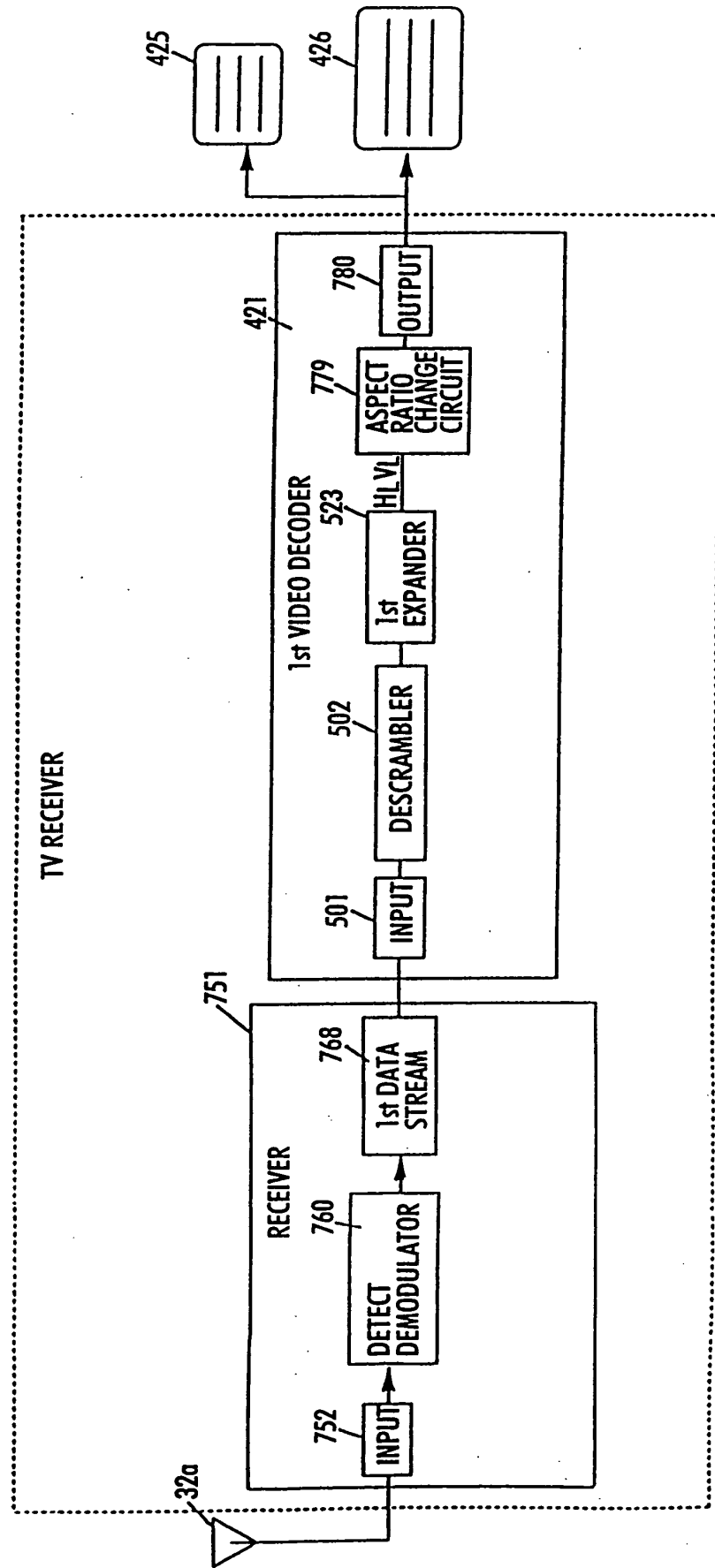


FIG. 67

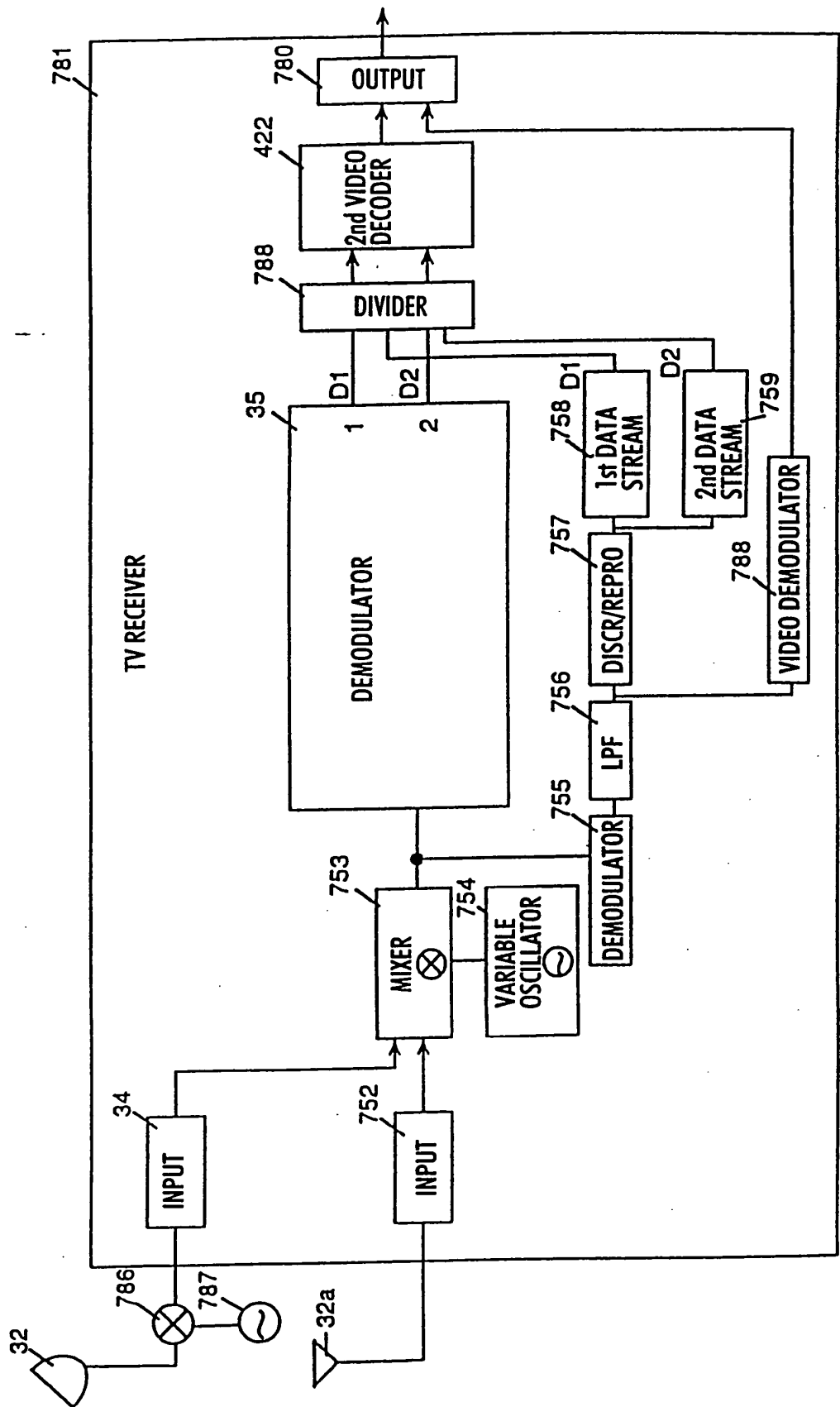


FIG. 68

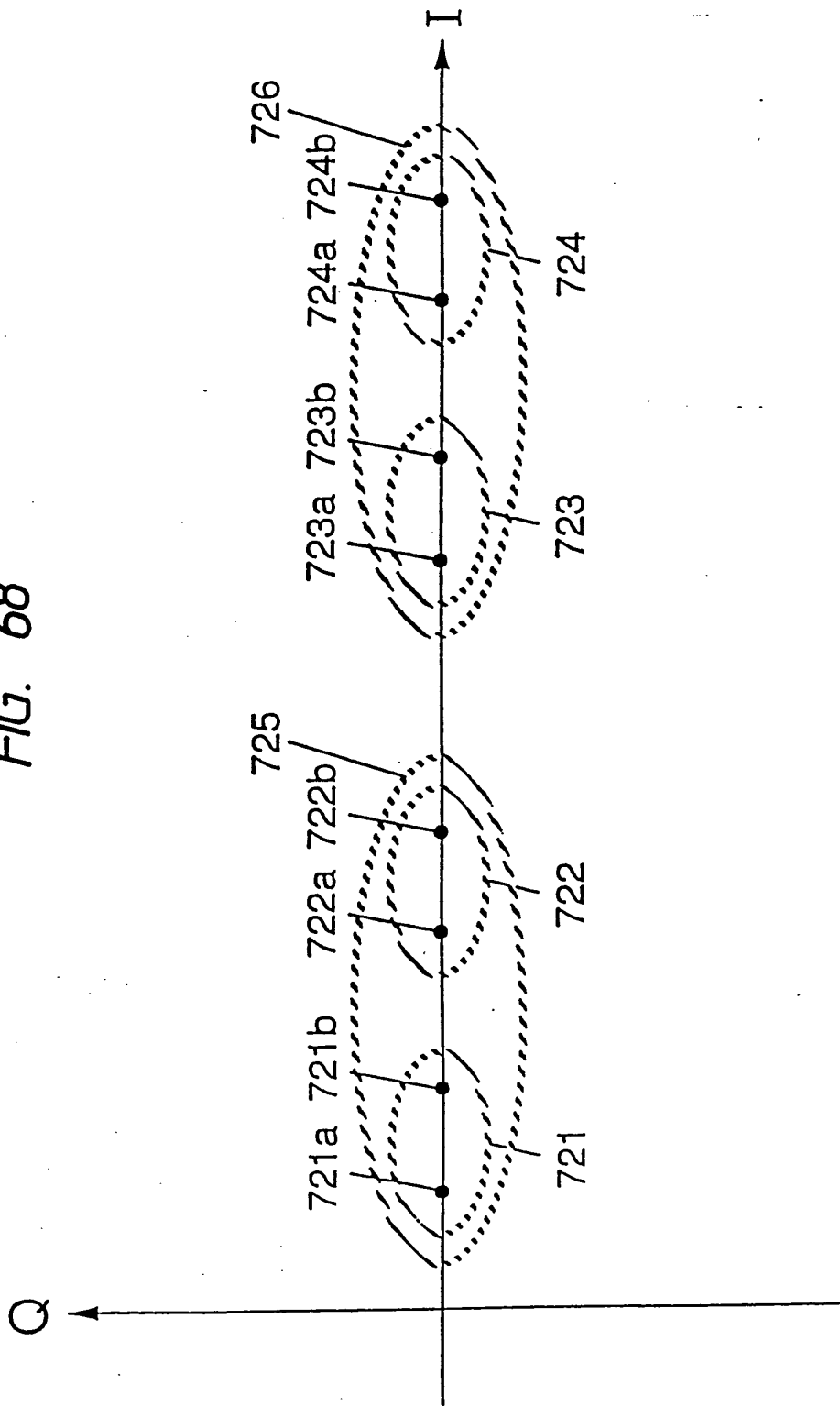


FIG. 69

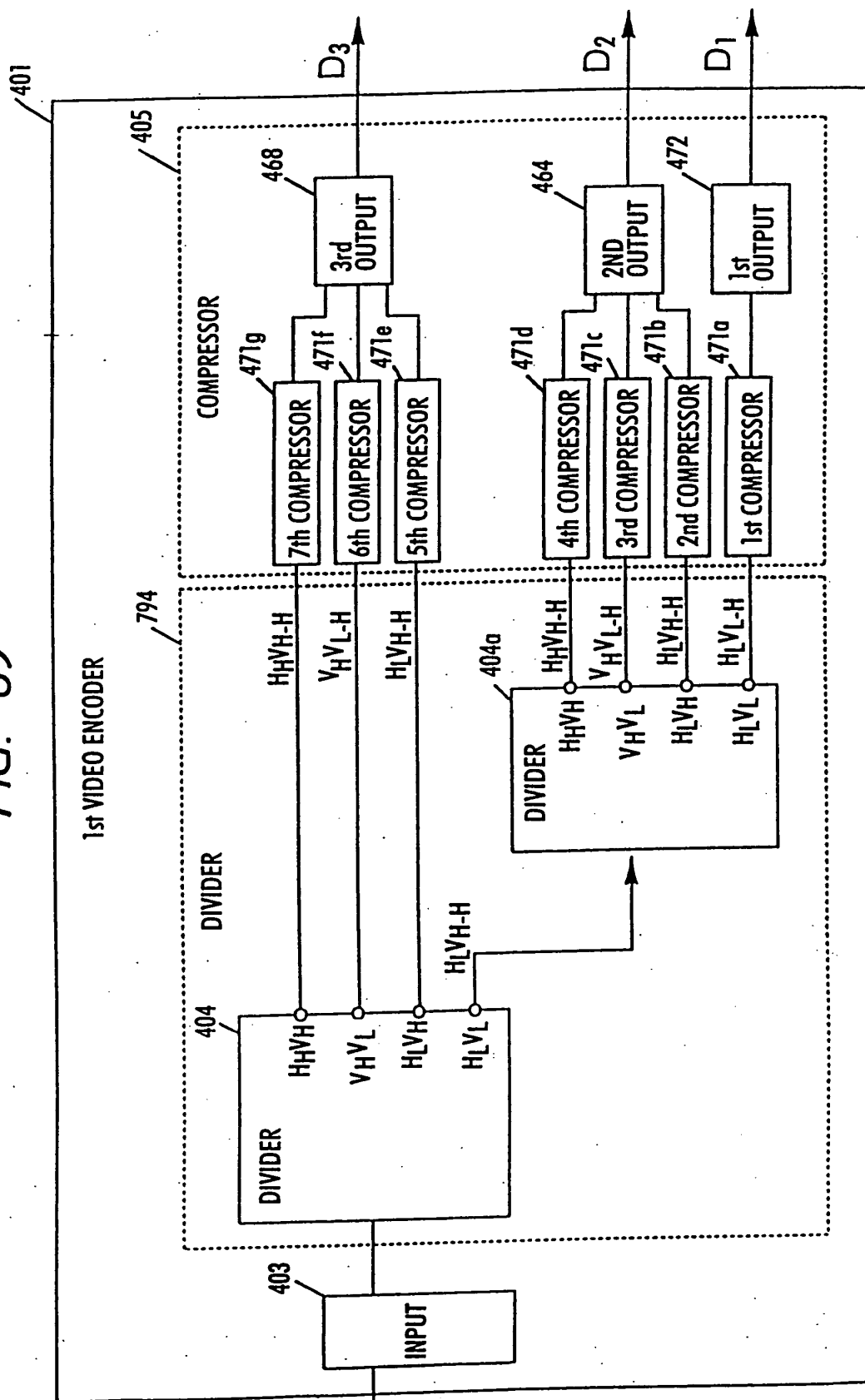


FIG. 70

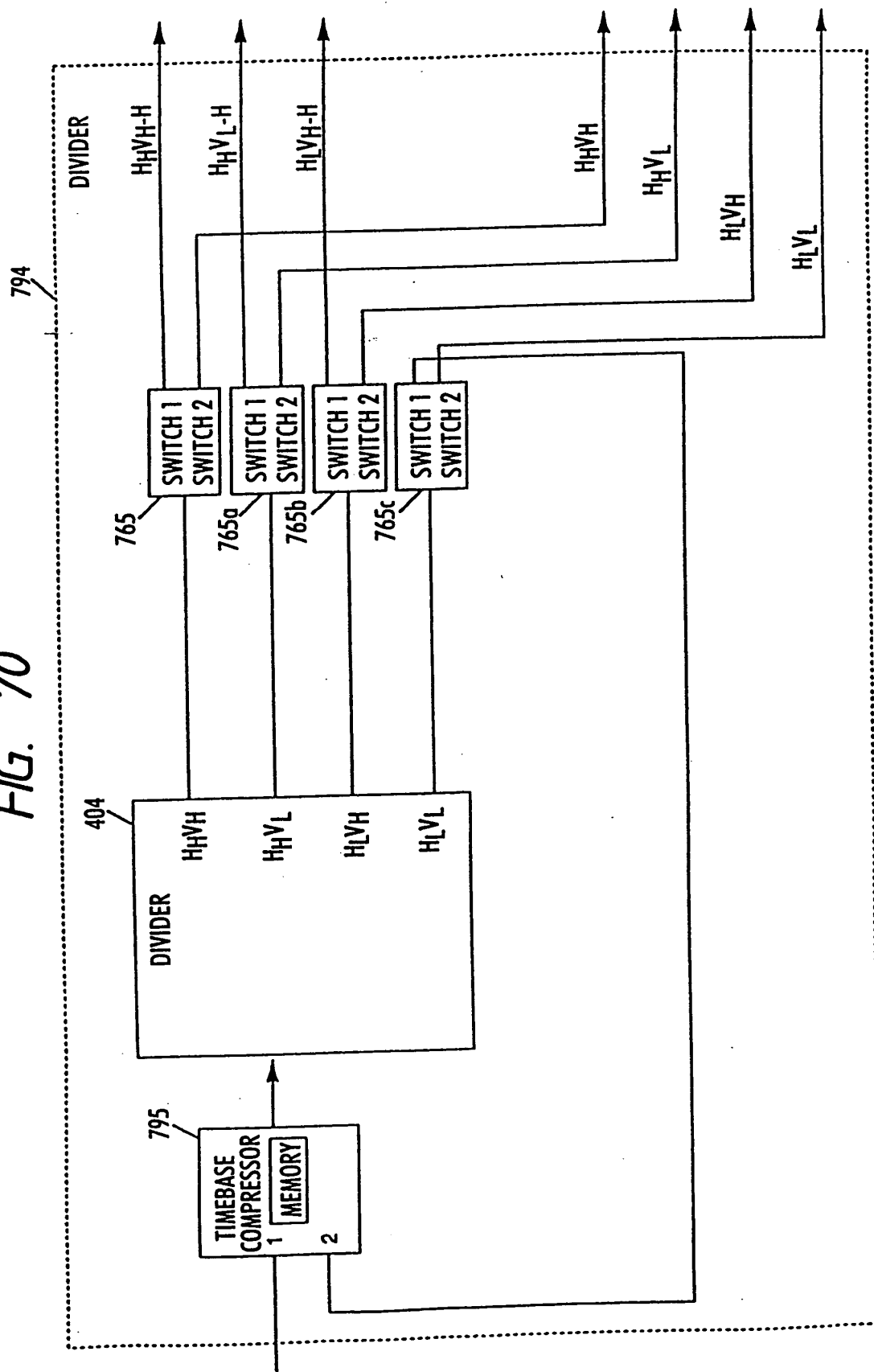


FIG. 71

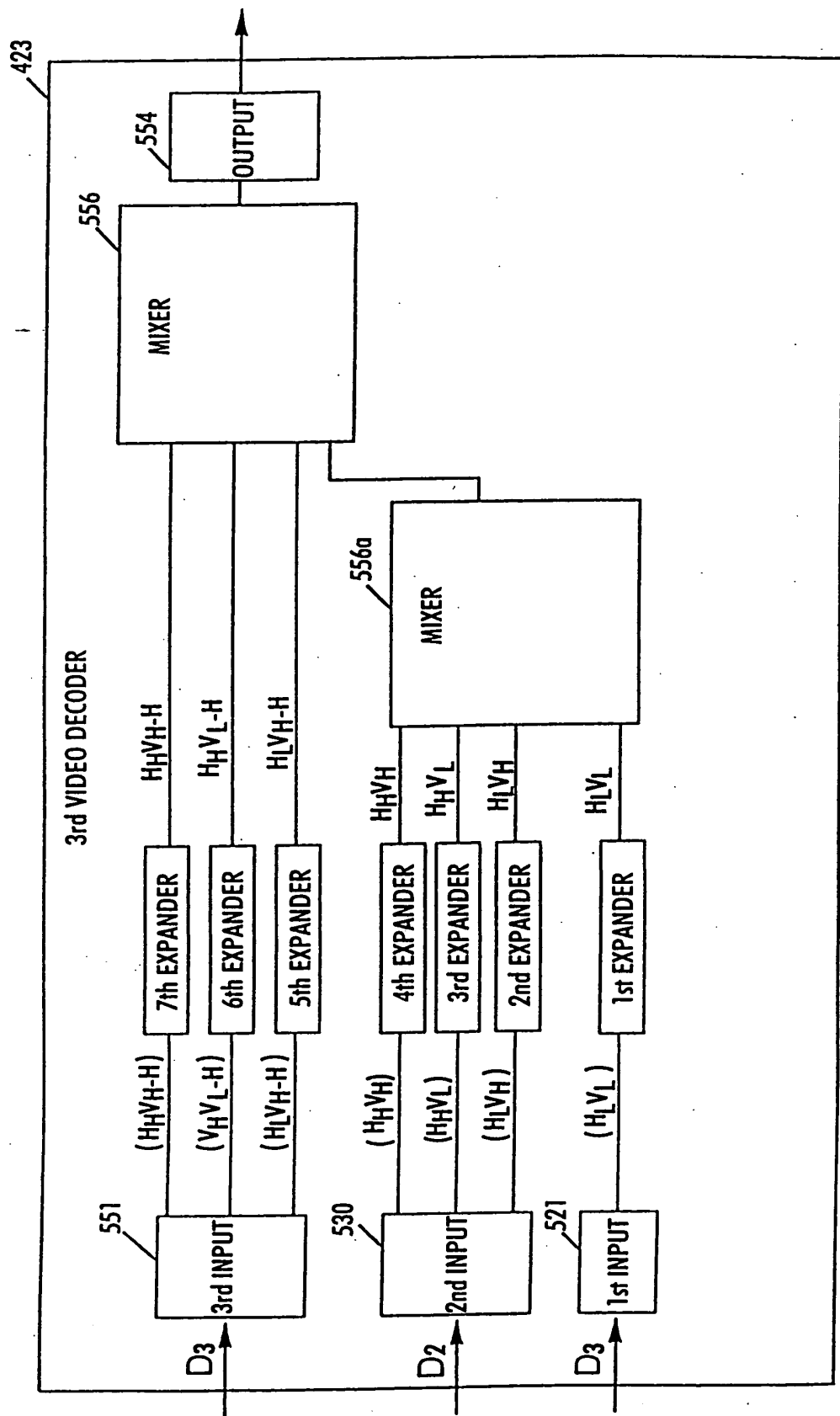


FIG. 72

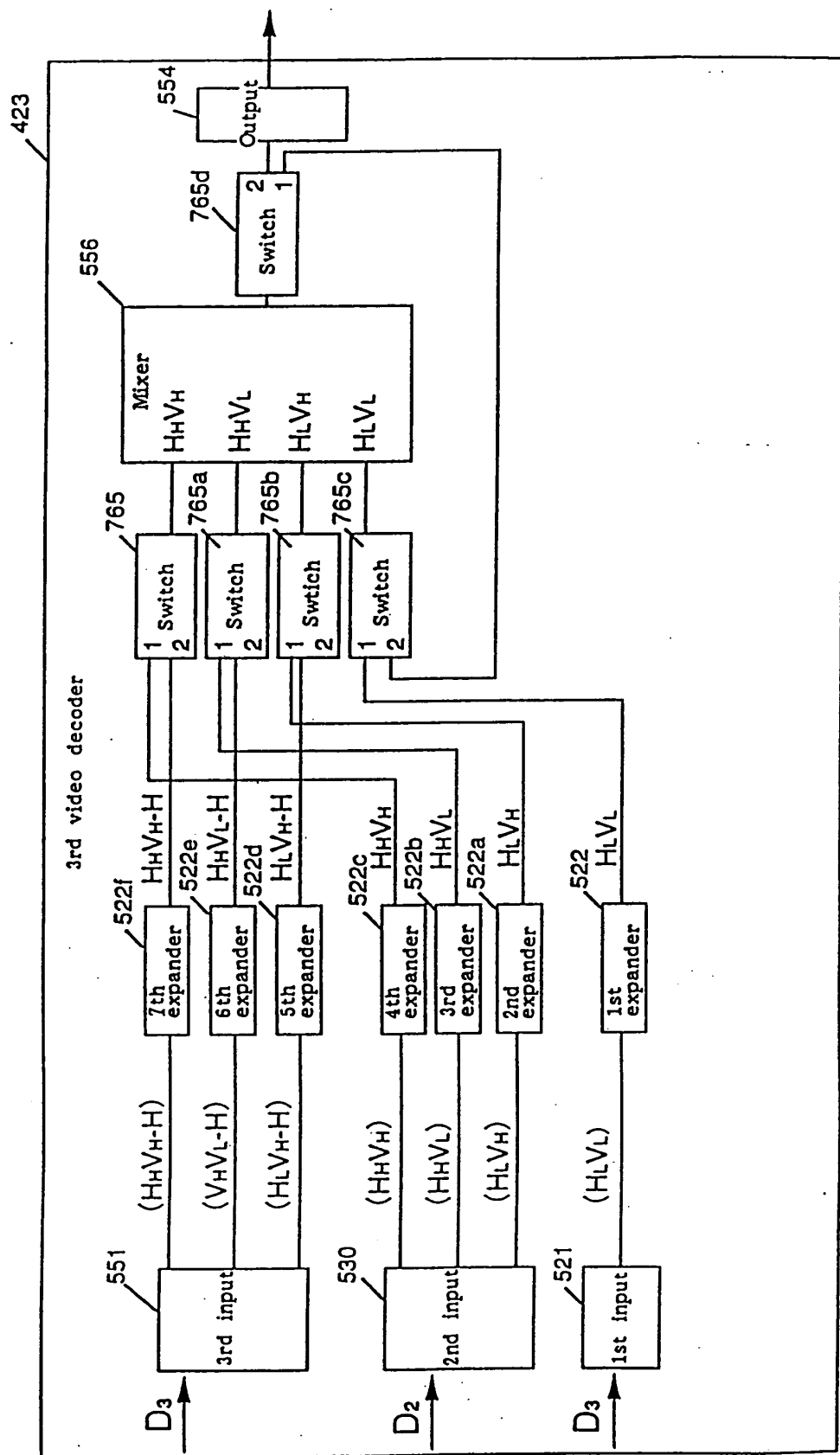


FIG. 73

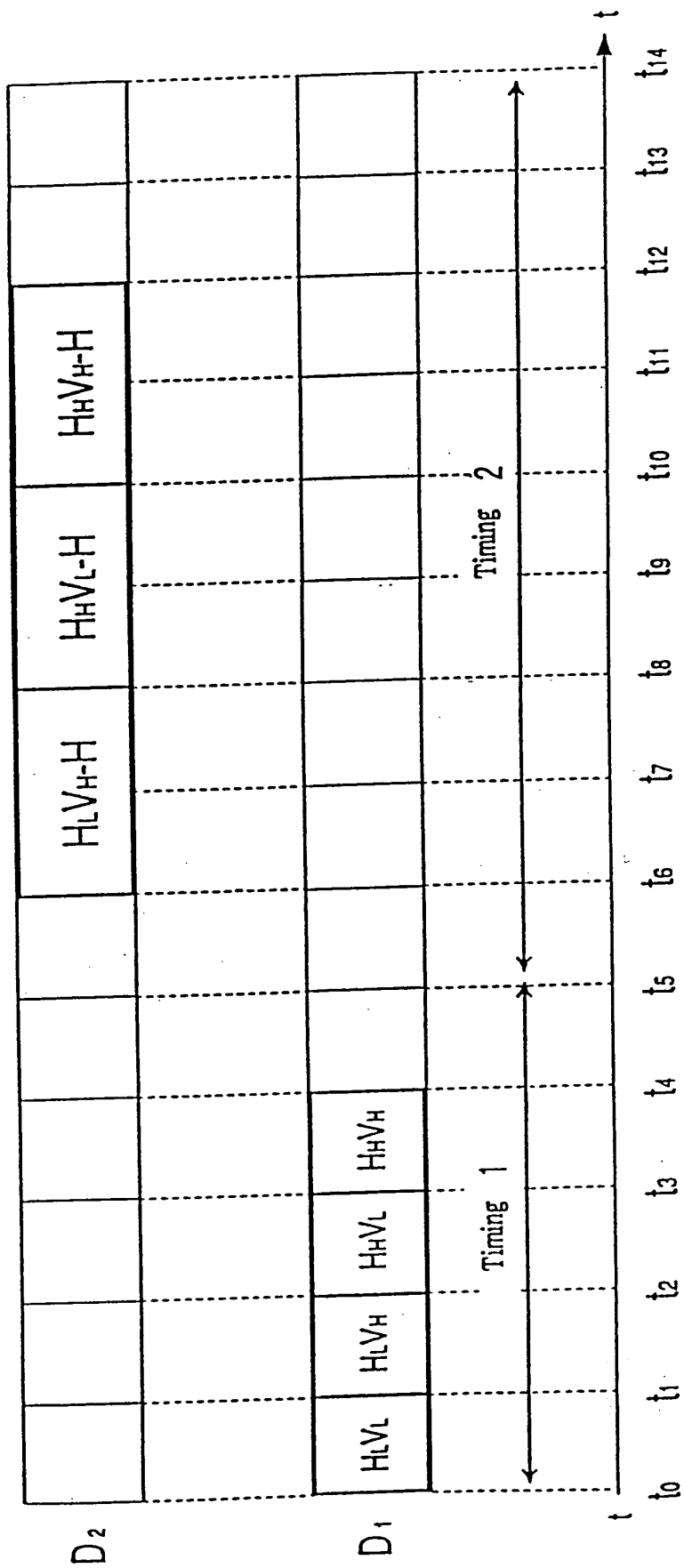


FIG. 74 (a)

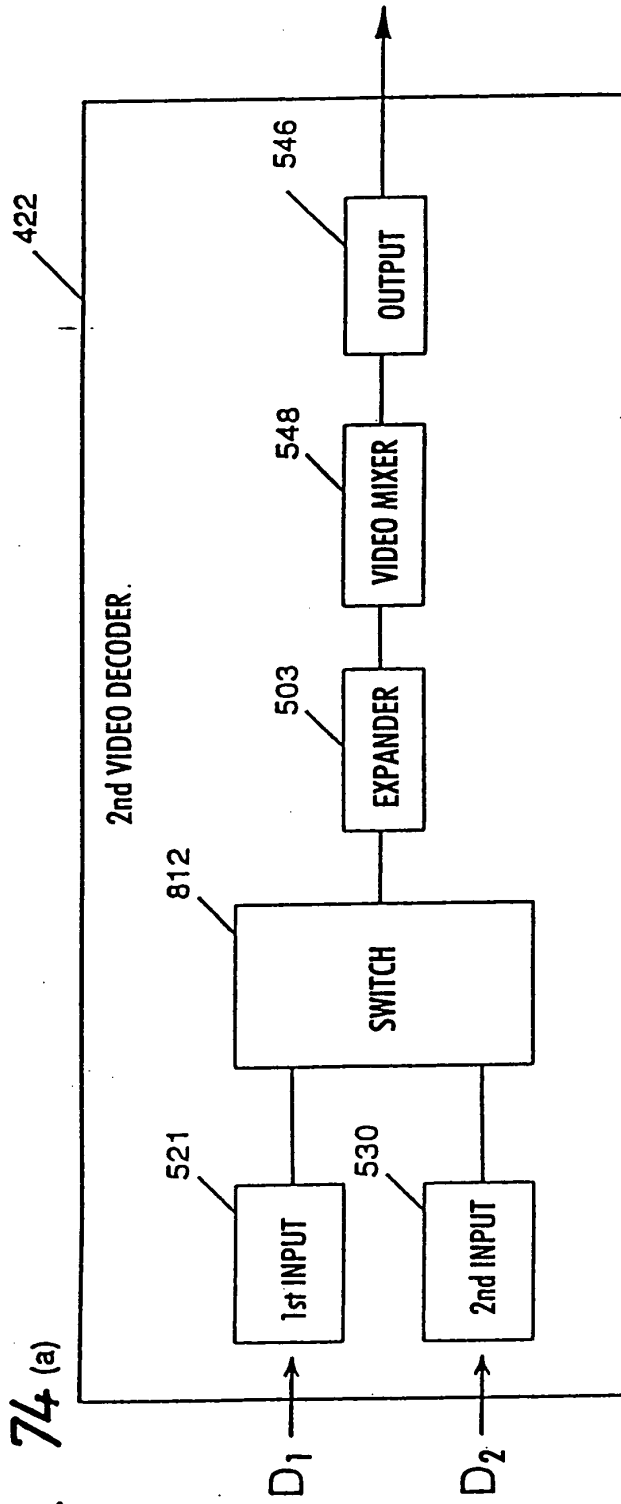


FIG. 74 (b)

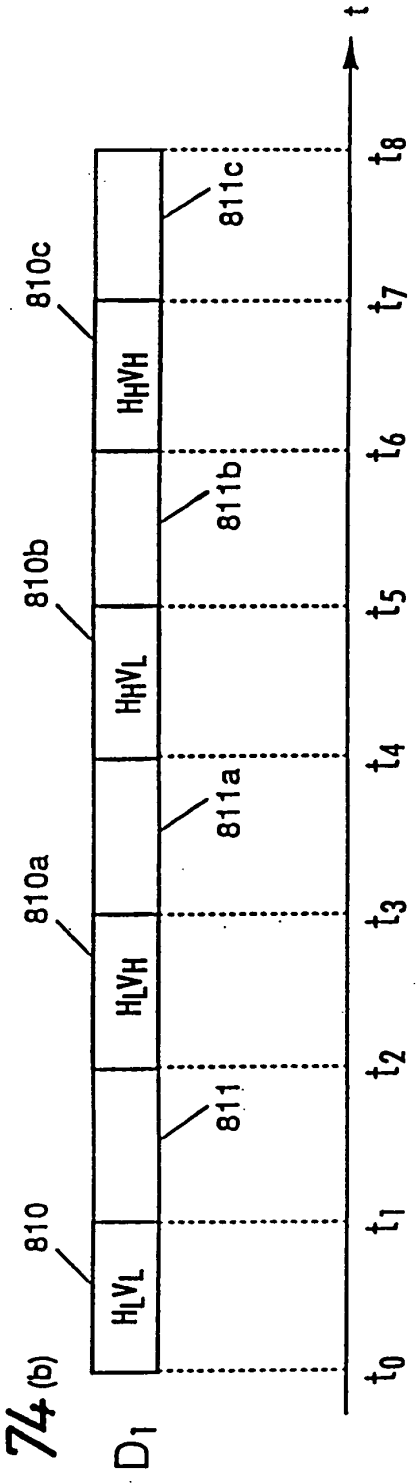


FIG. 75

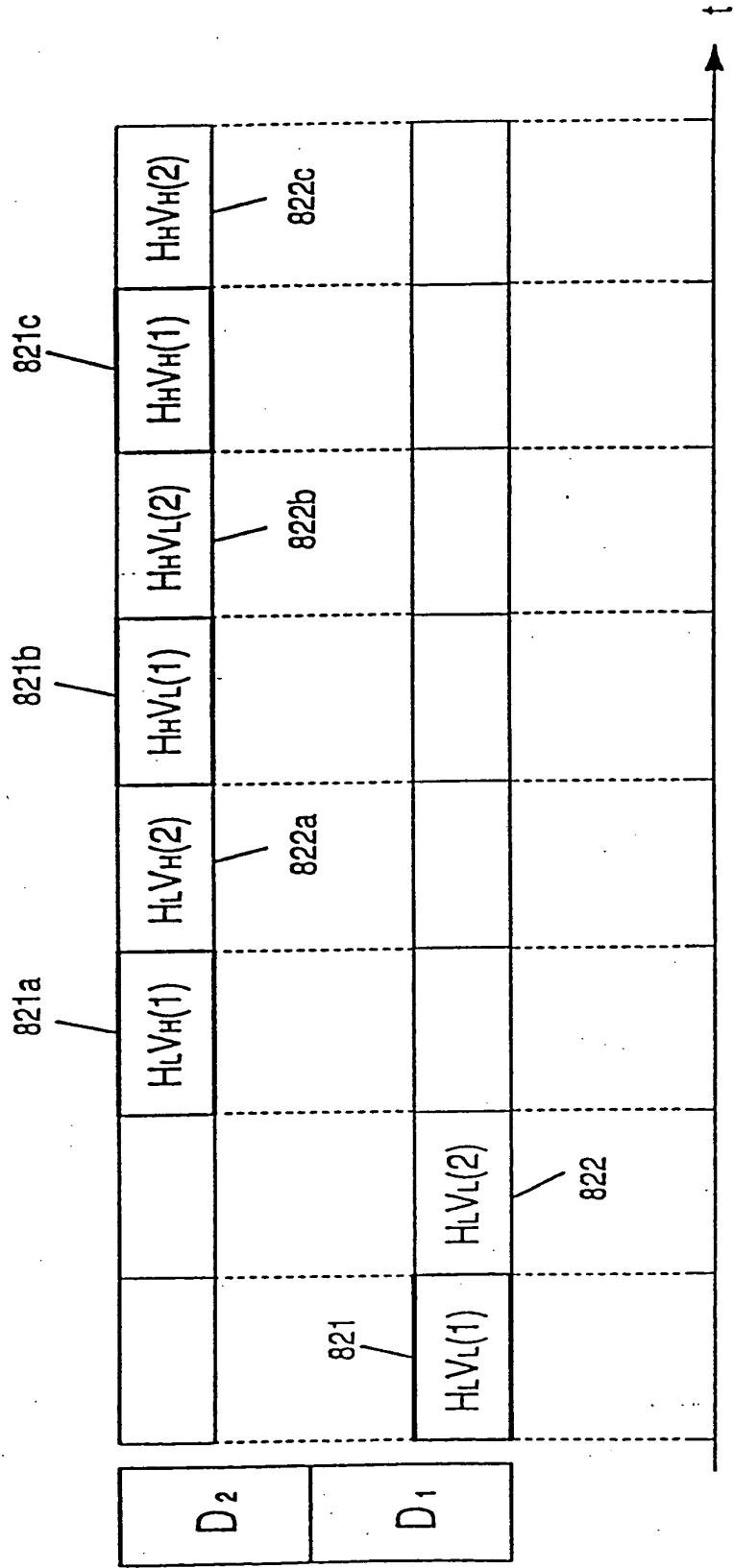
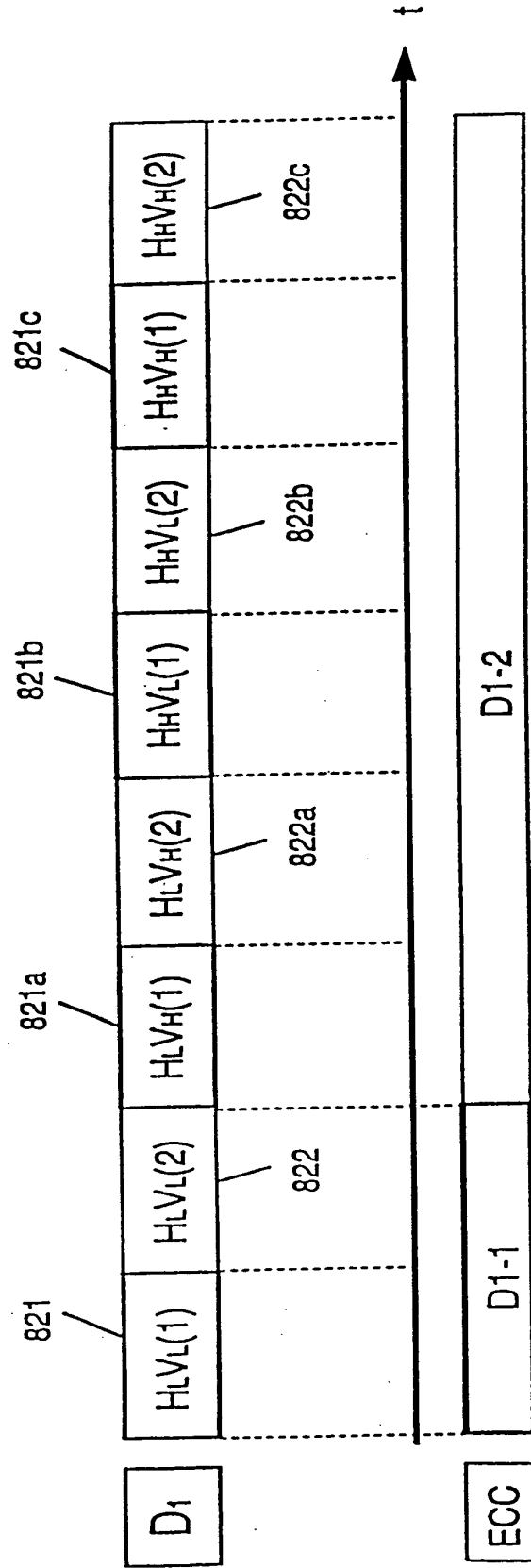


FIG. 76



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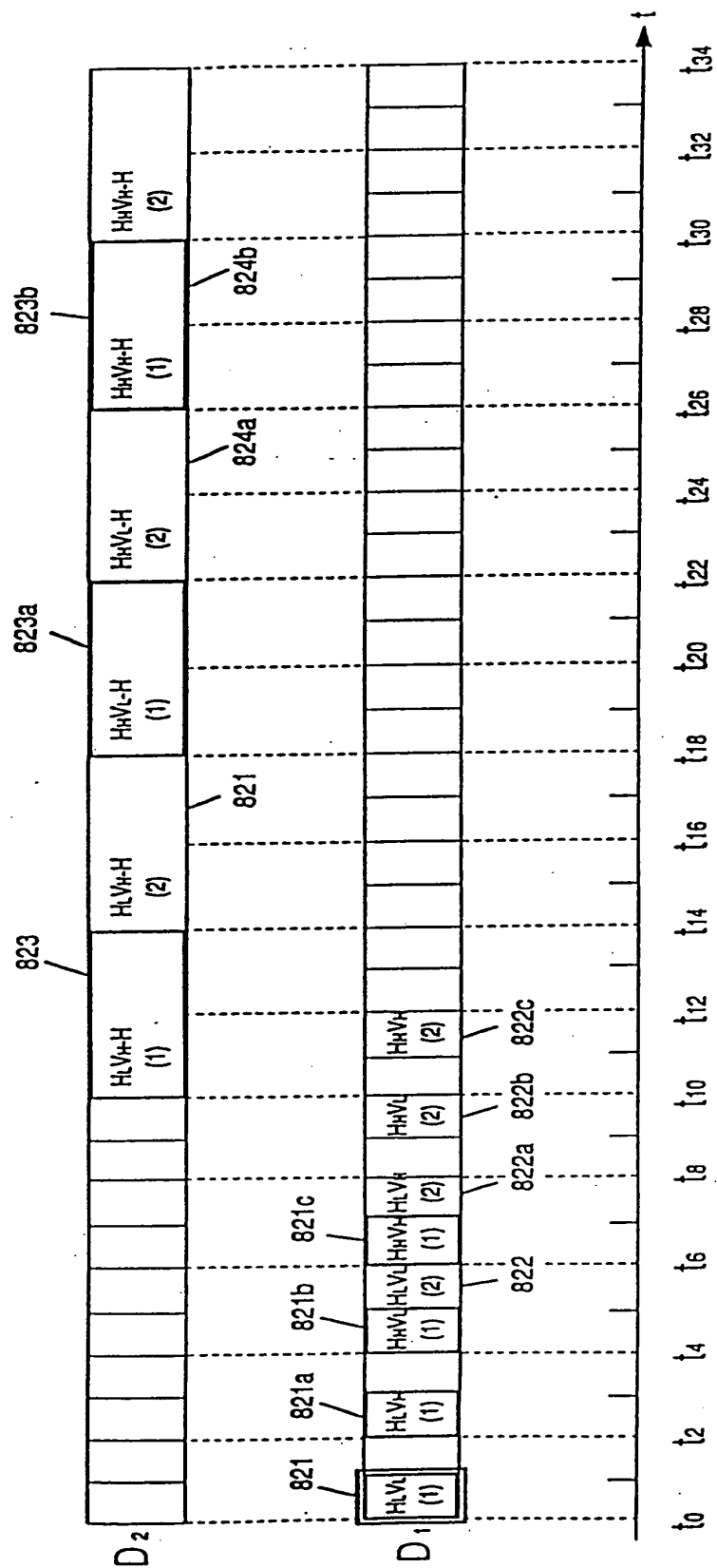


FIG. 78

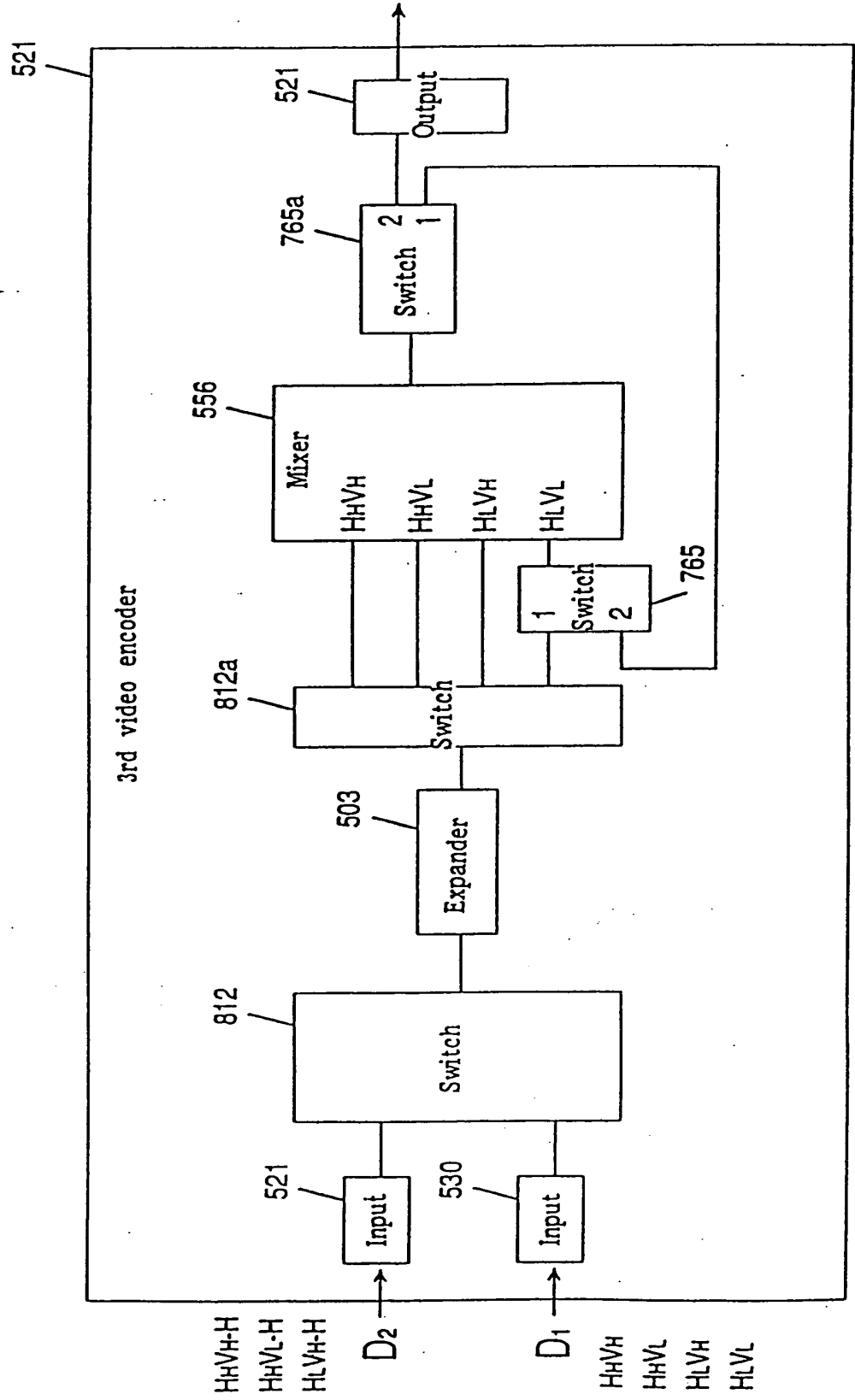


FIG. 79

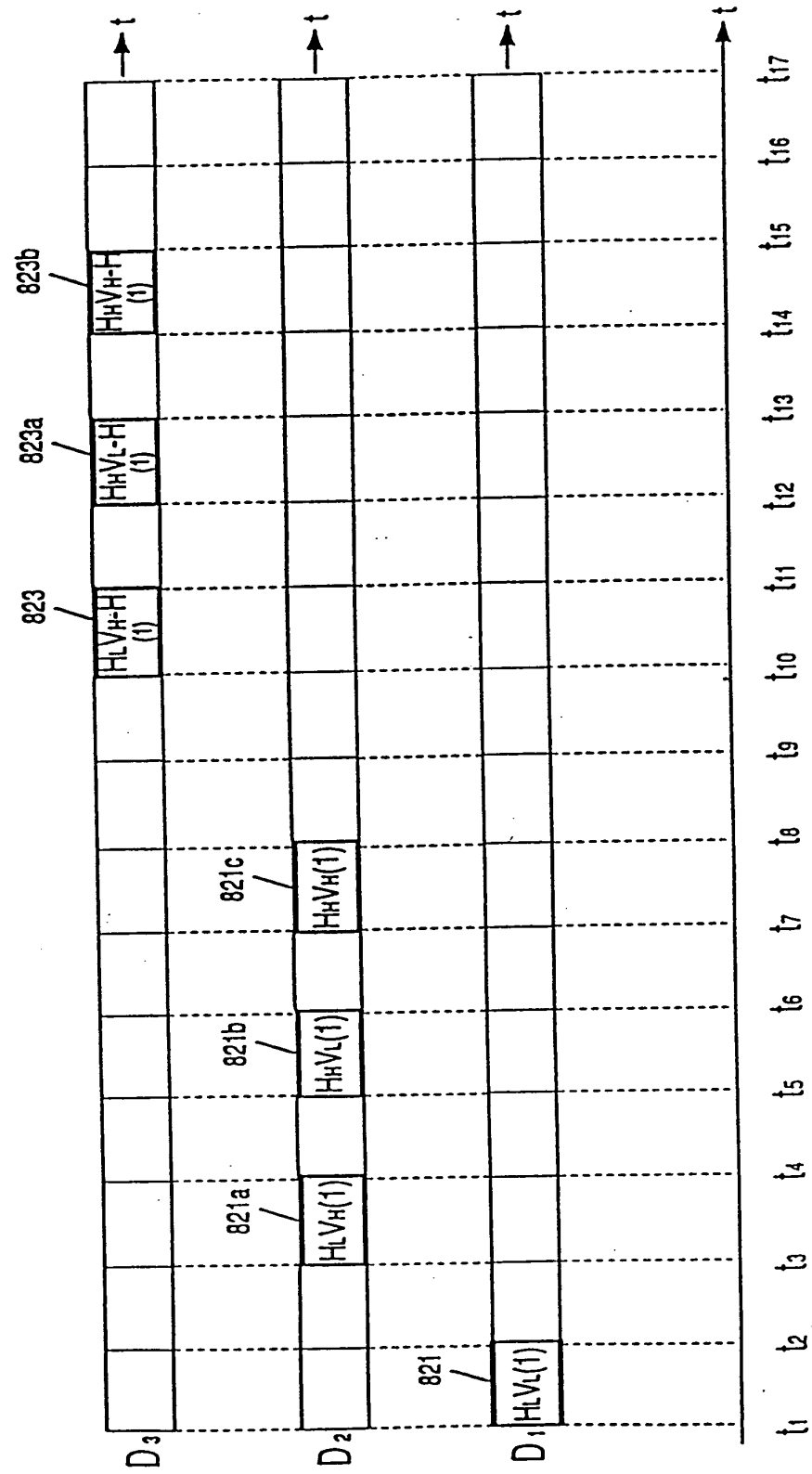


FIG. 80

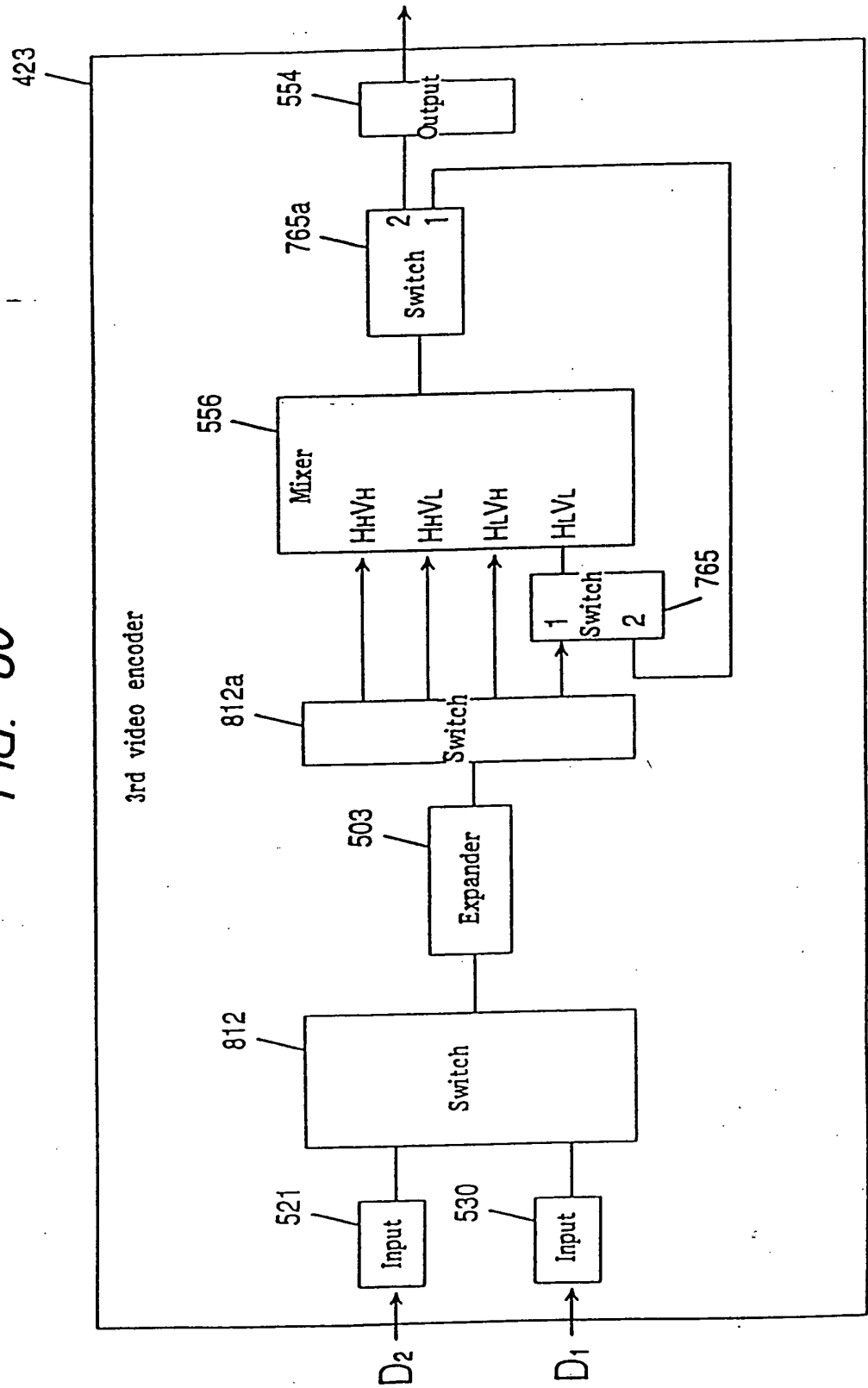


FIG. 81

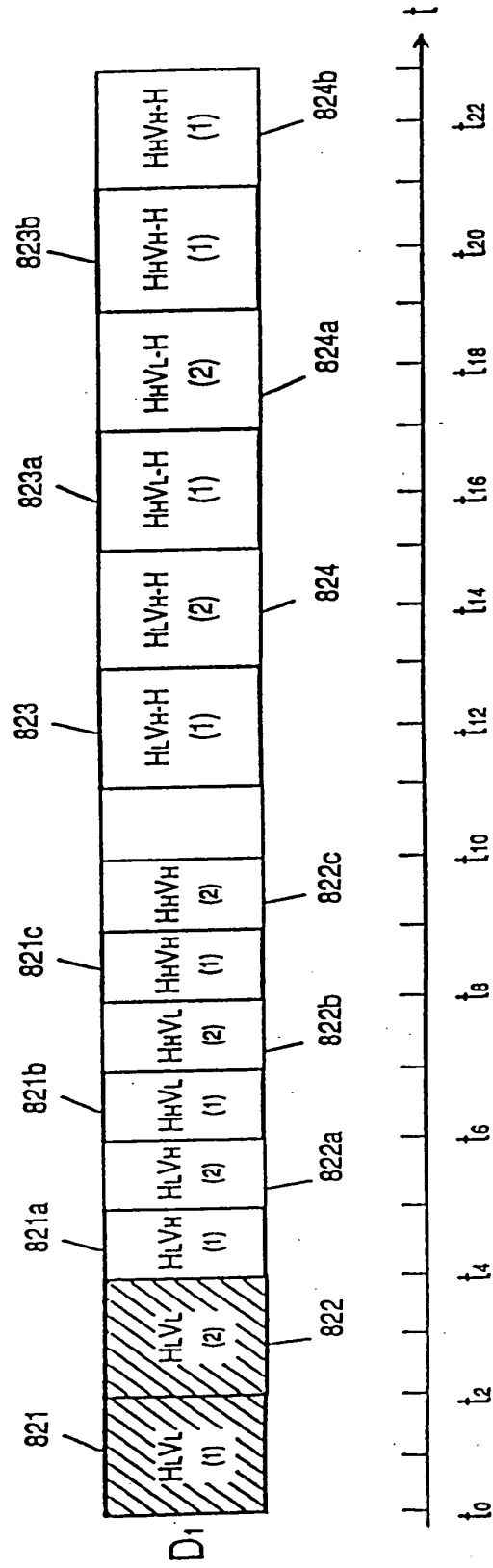


FIG. 82

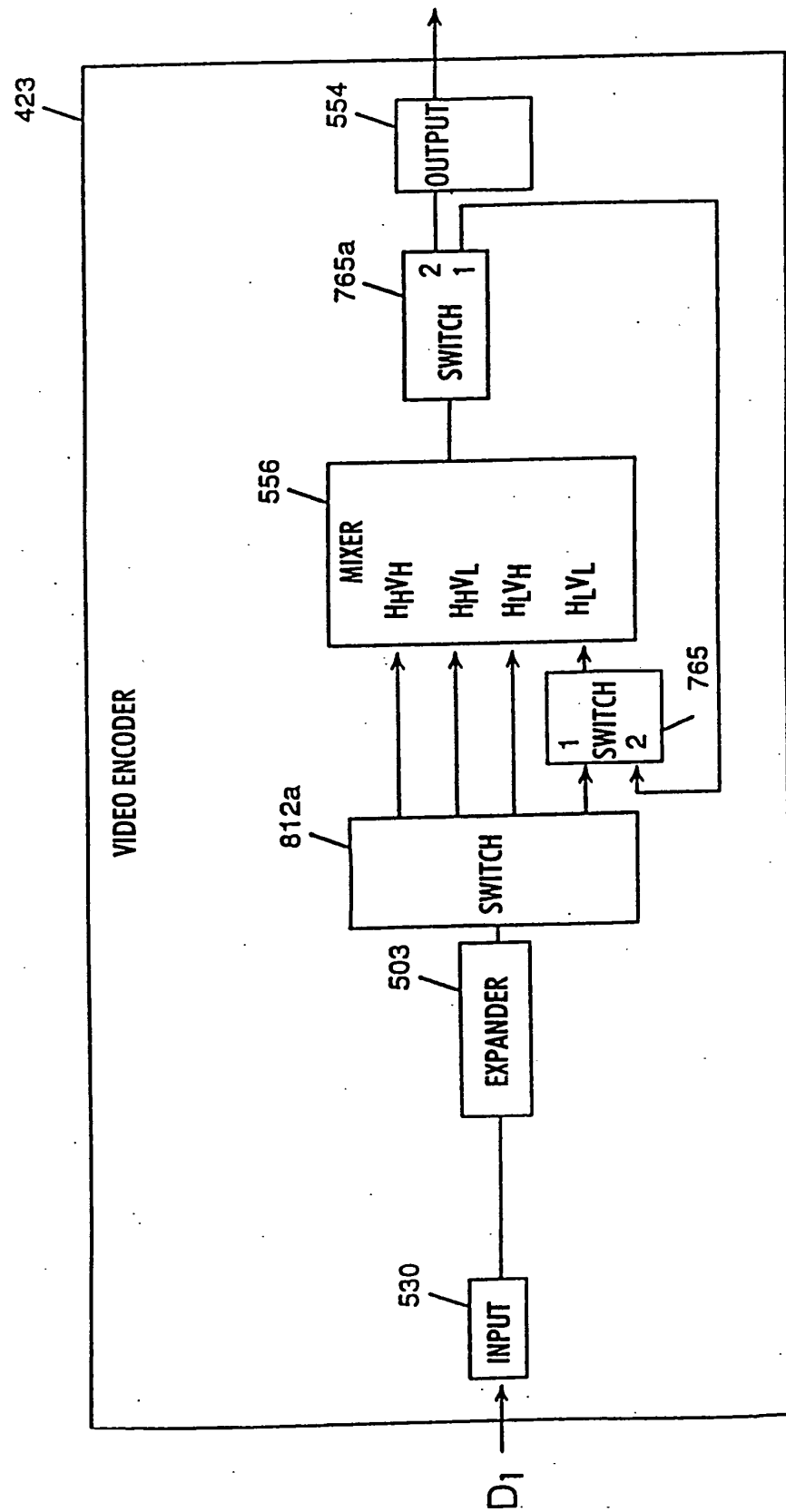


FIG. 83

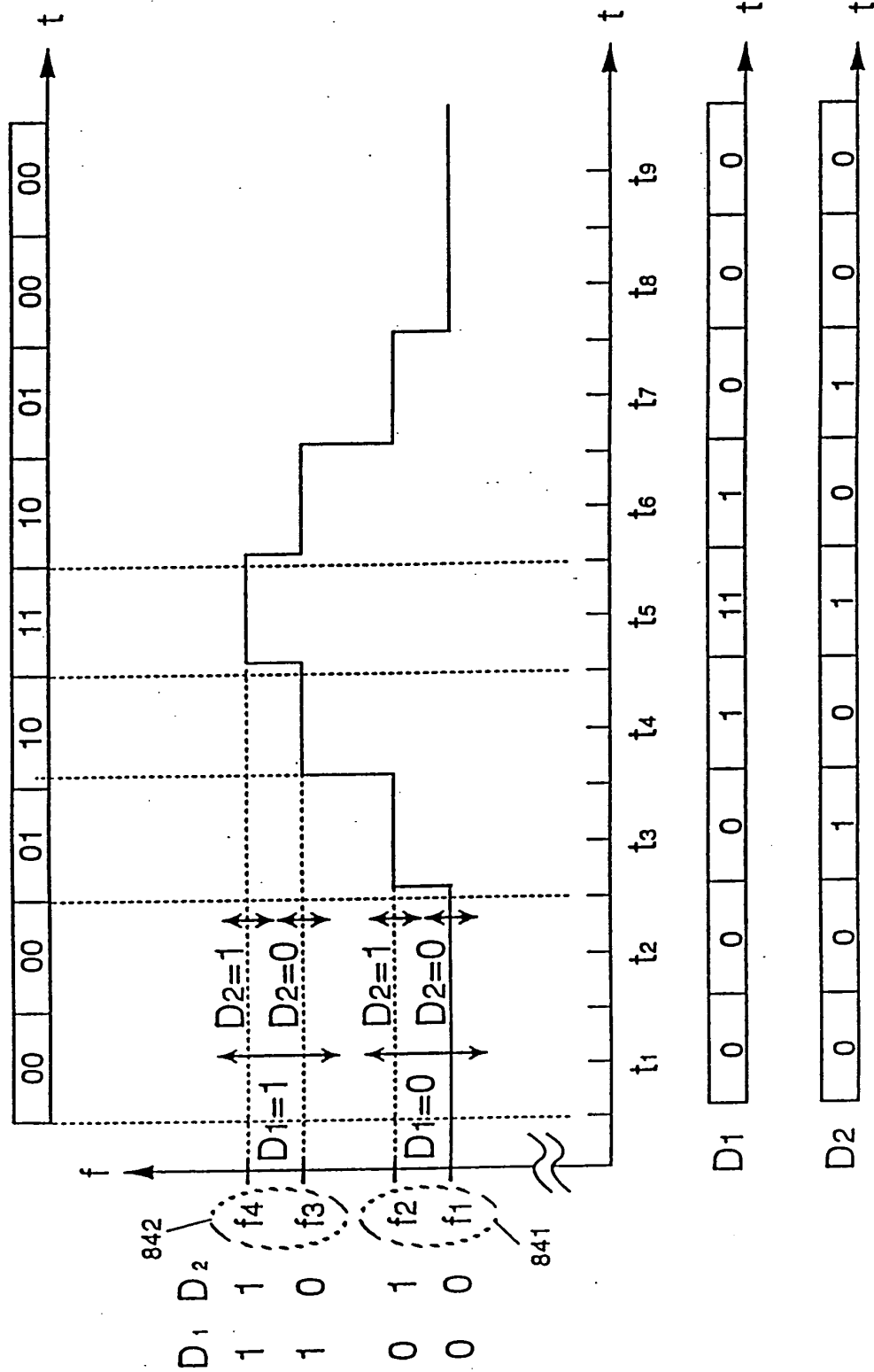


FIG. 84

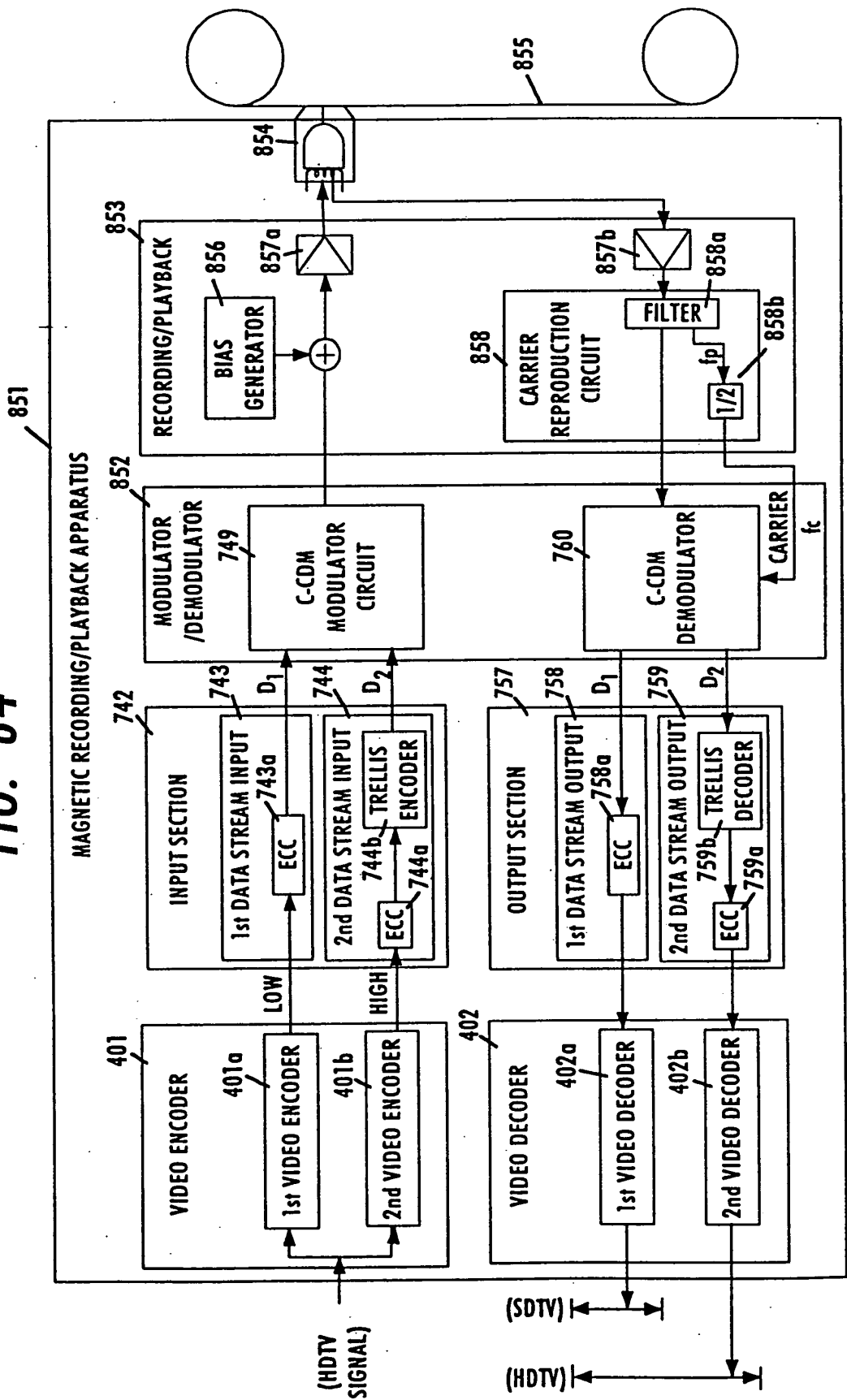


FIG. 85

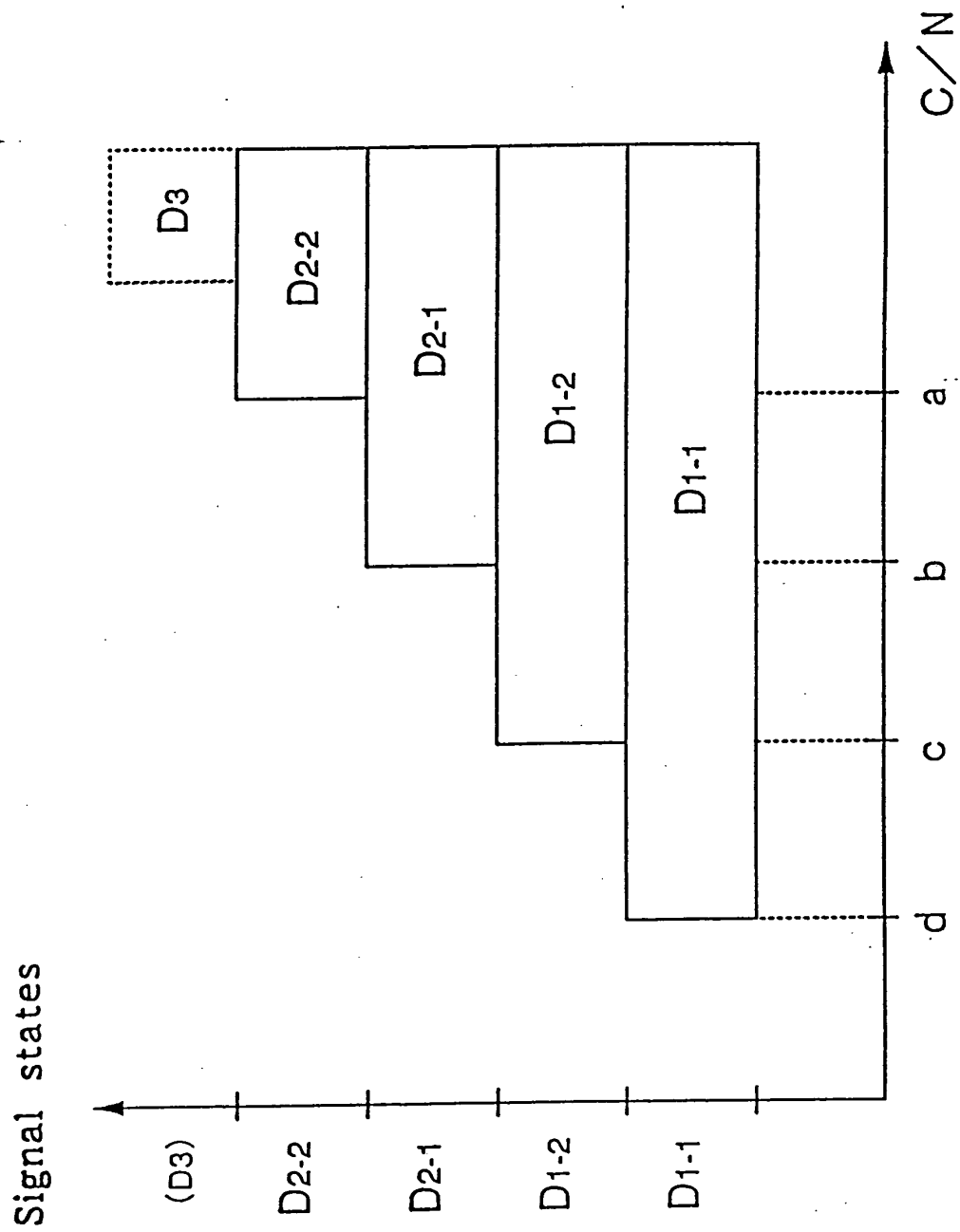


FIG. 86

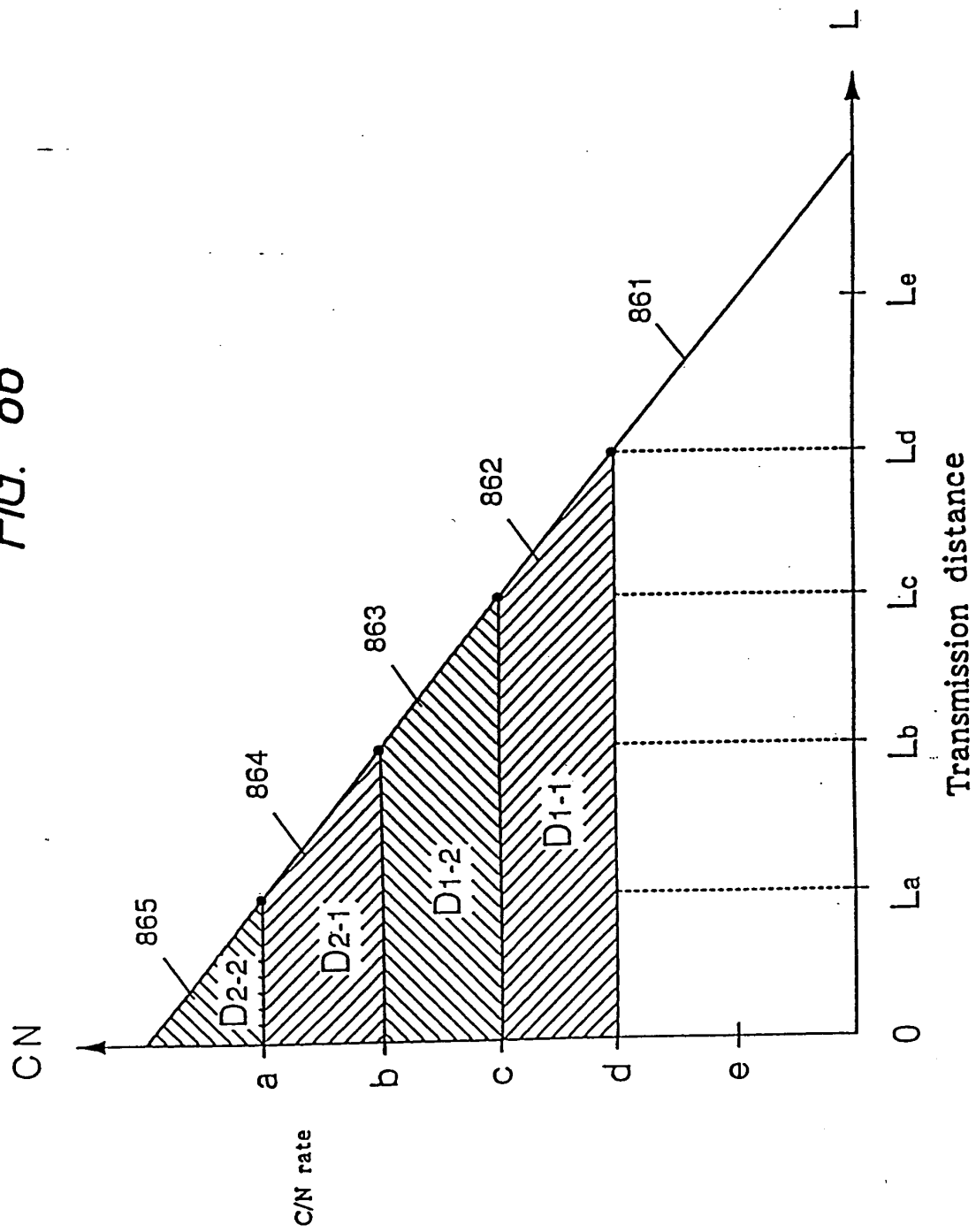


FIG. 87

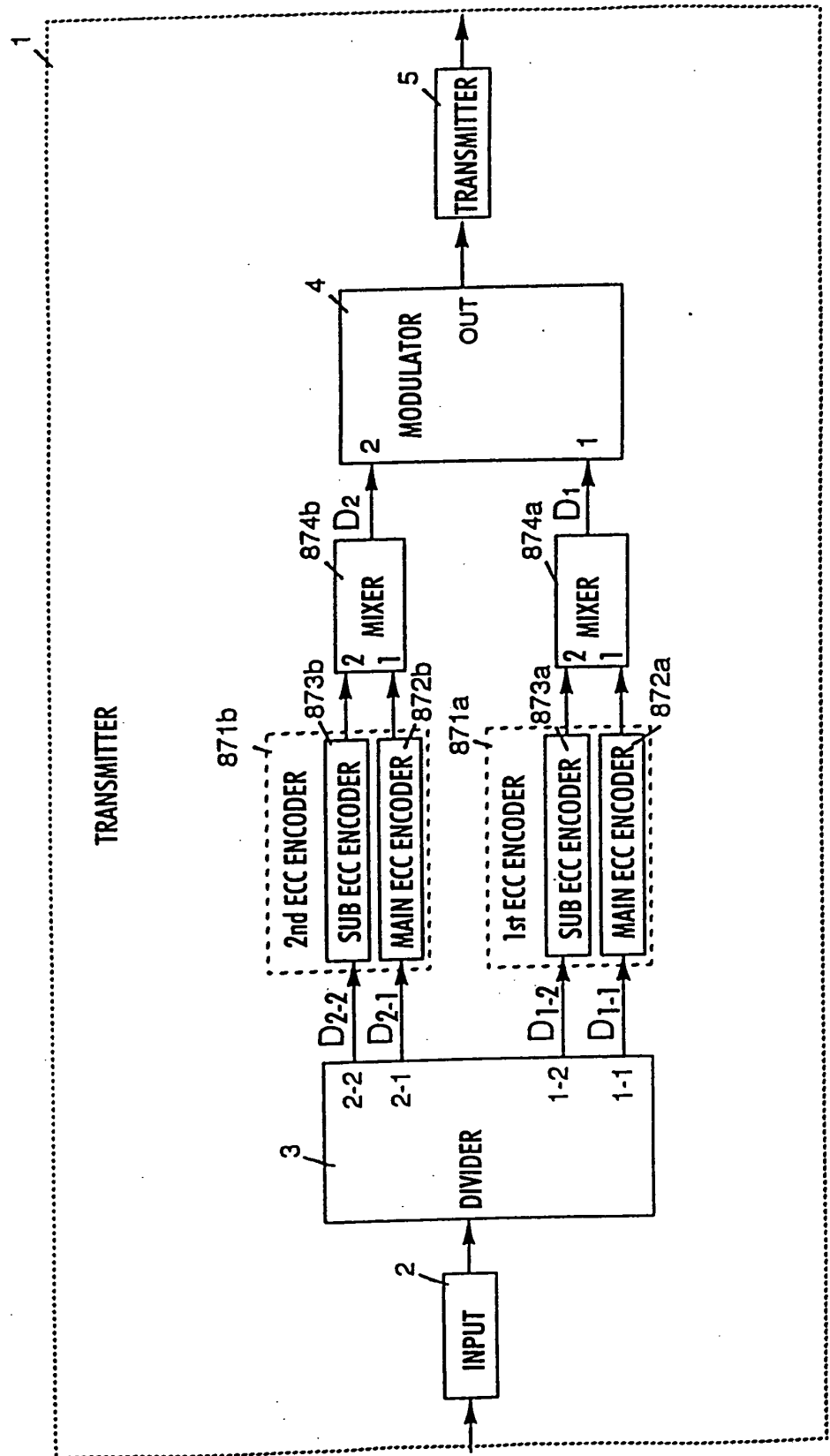


FIG. 88

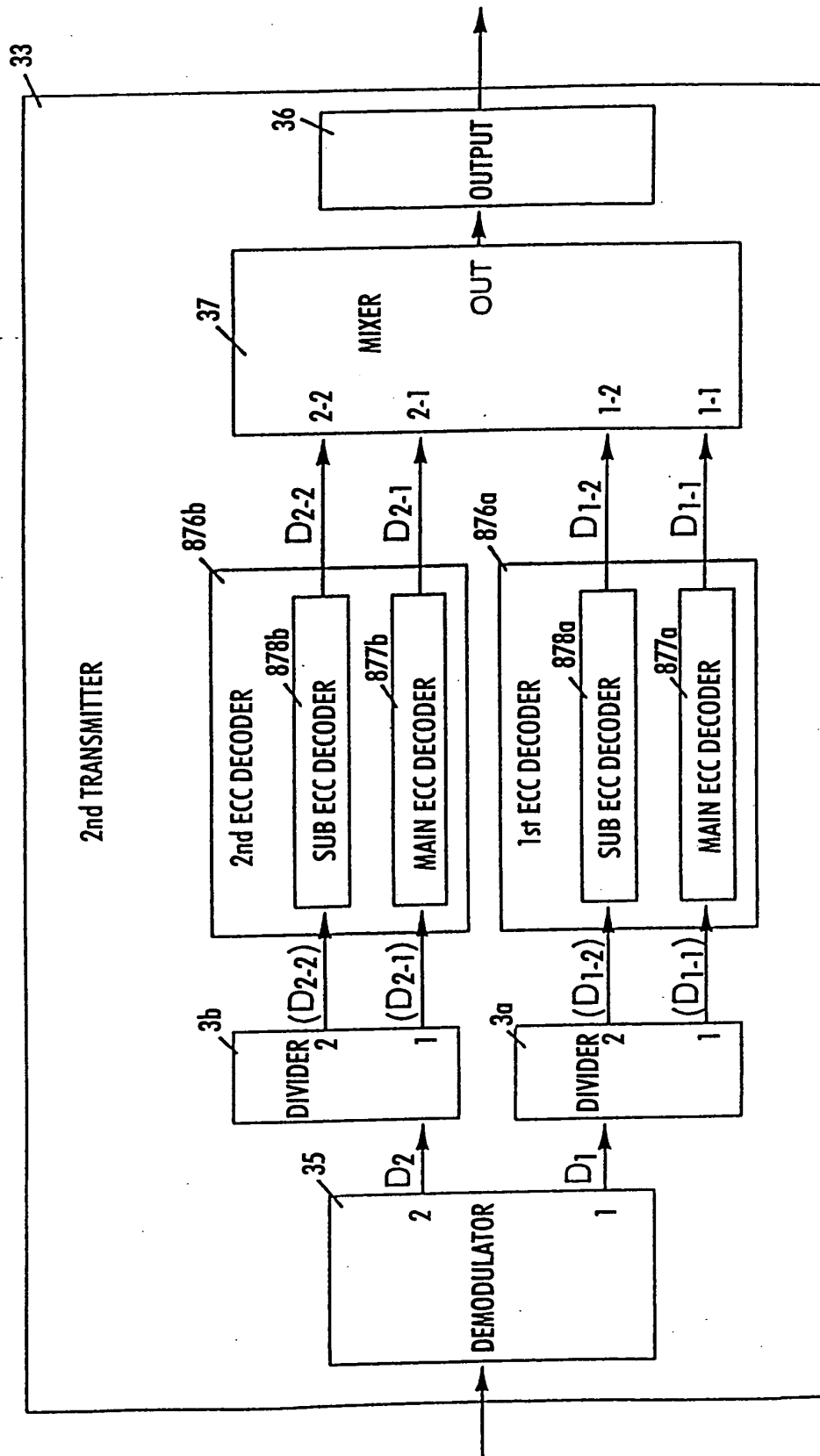


FIG. 89

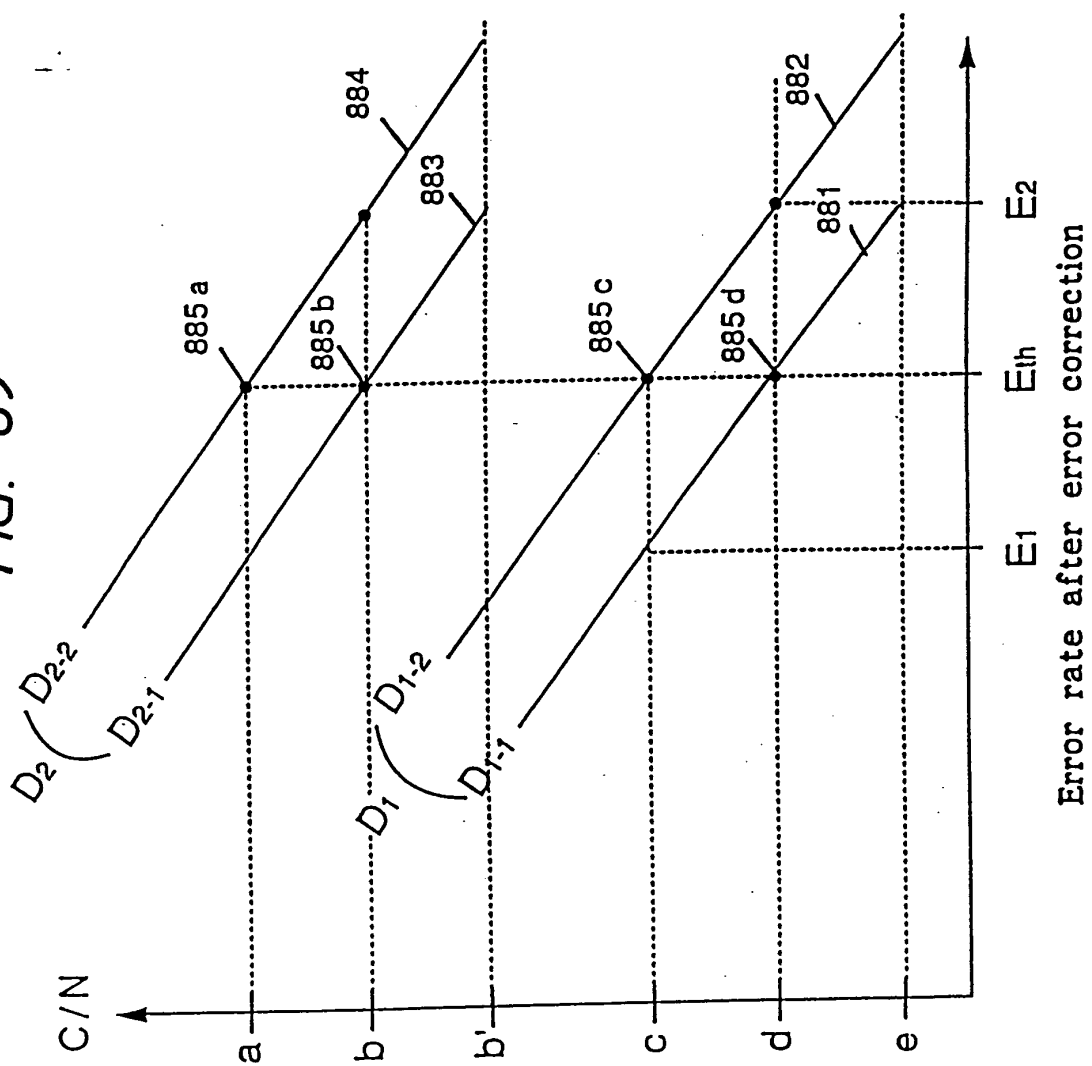


FIG. 90

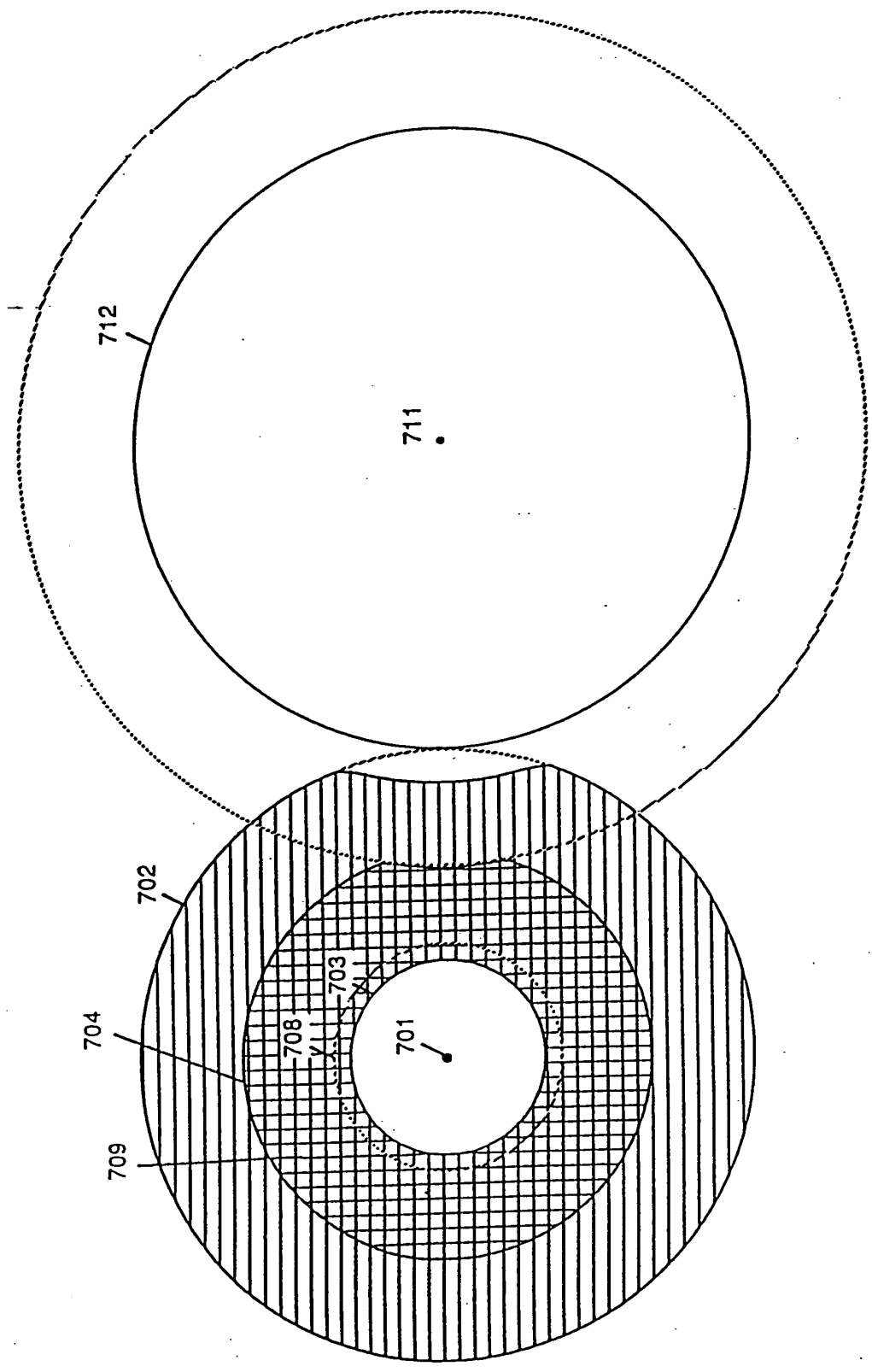


FIG. 91

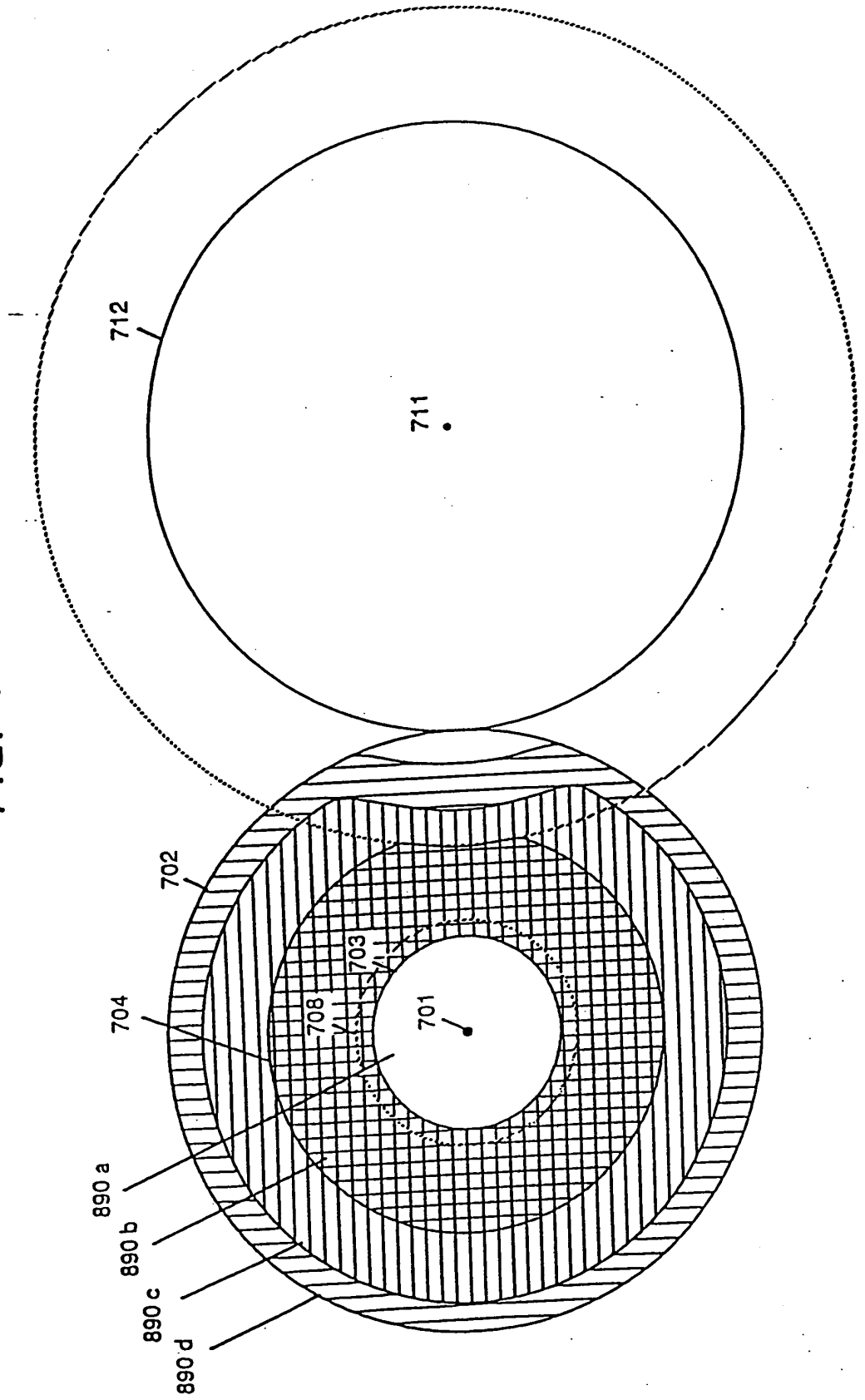


FIG. 92

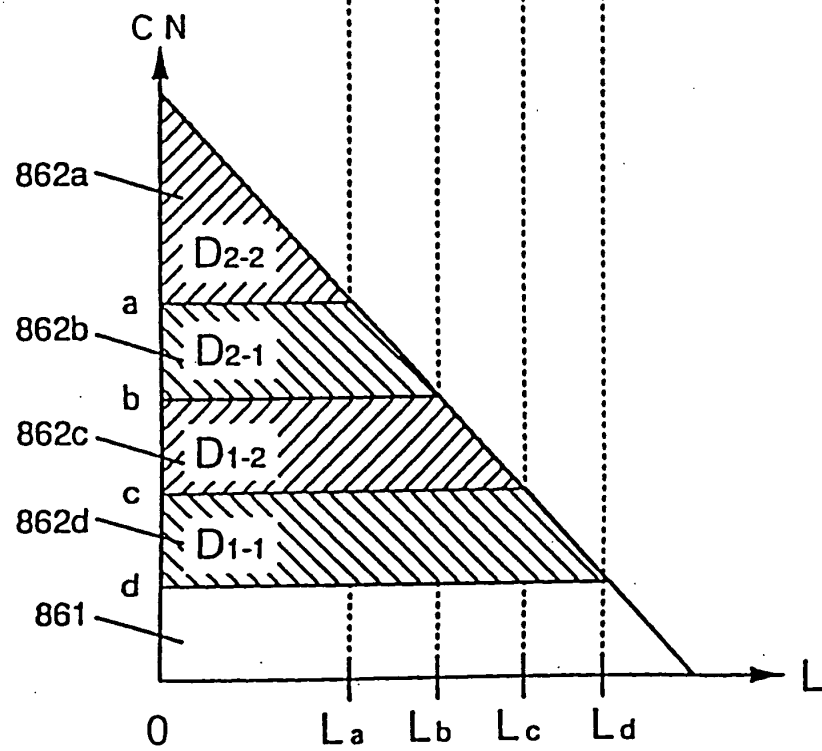
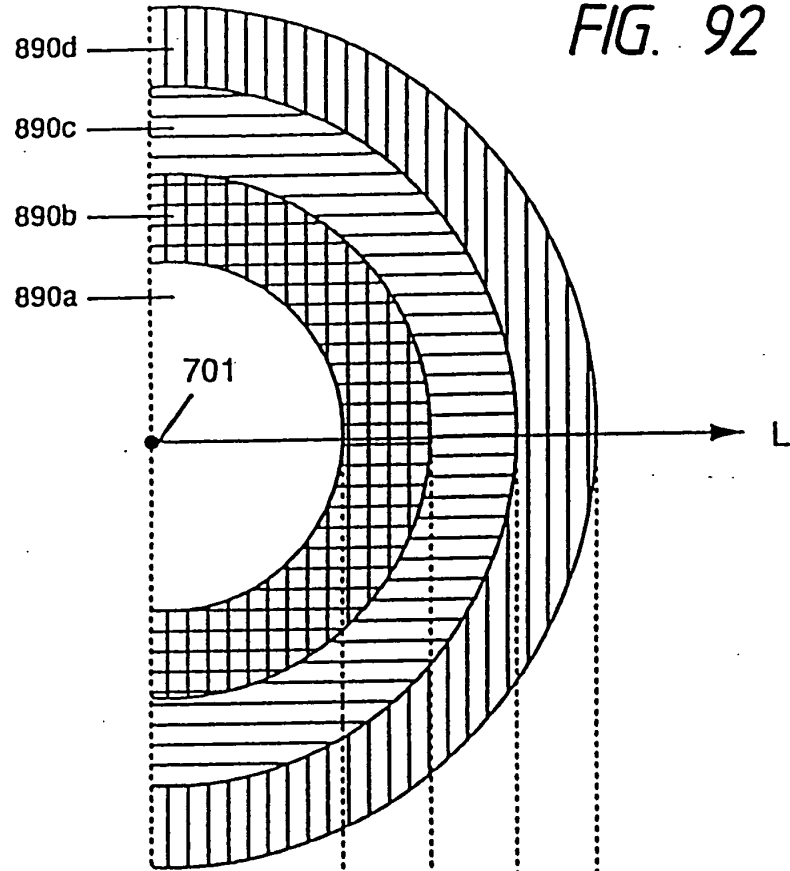


FIG. 93

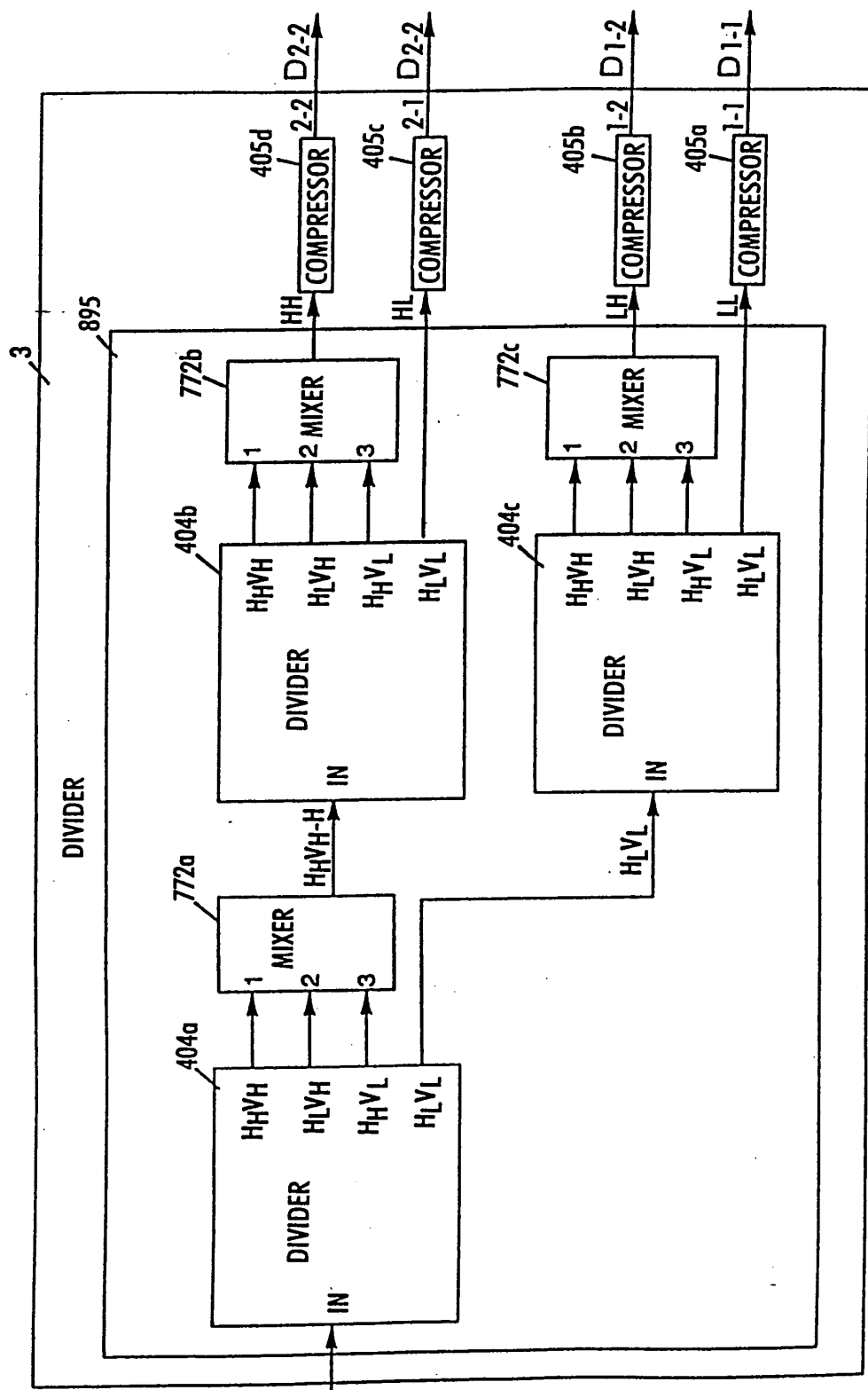


FIG. 94

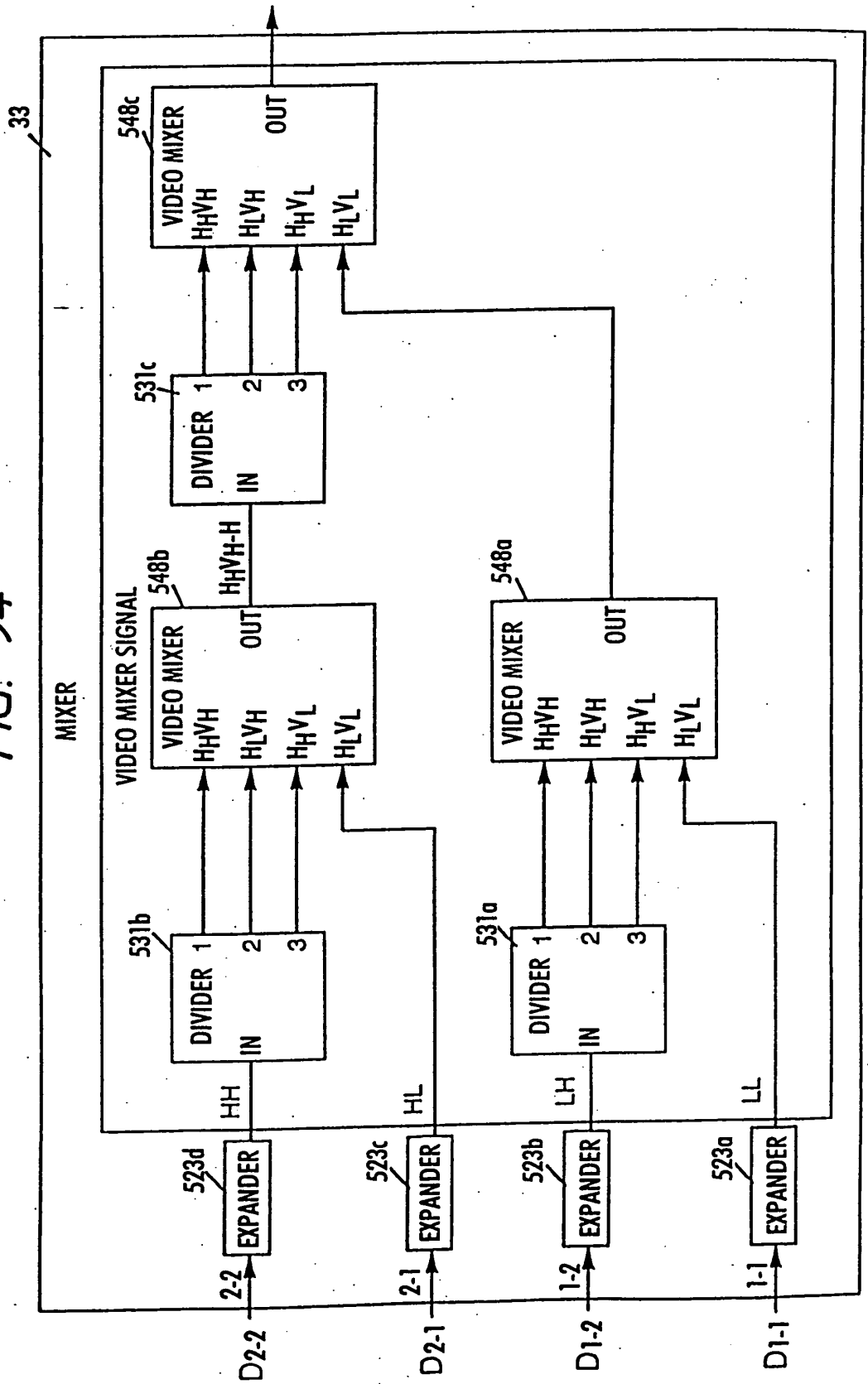


FIG. 95

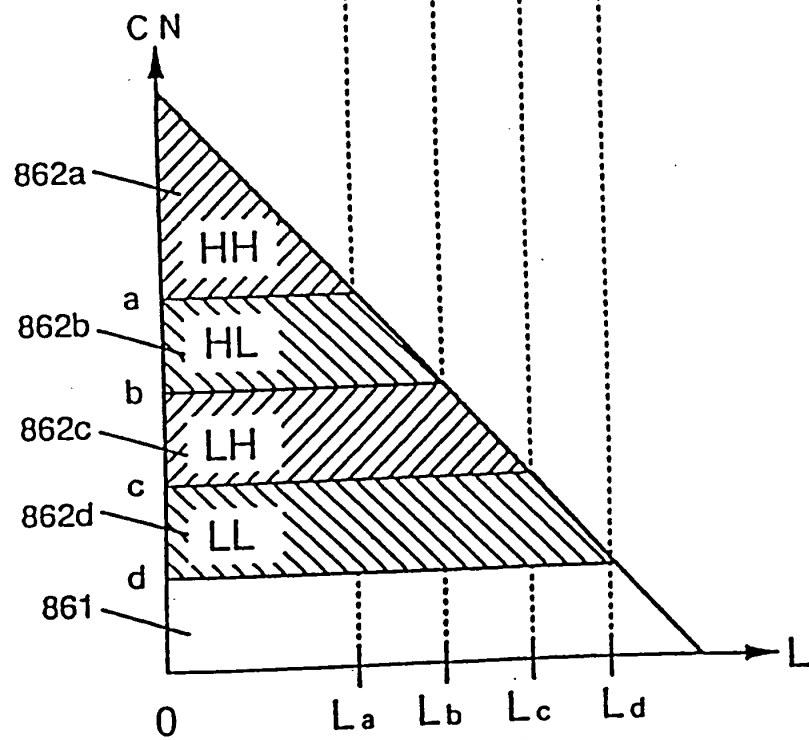
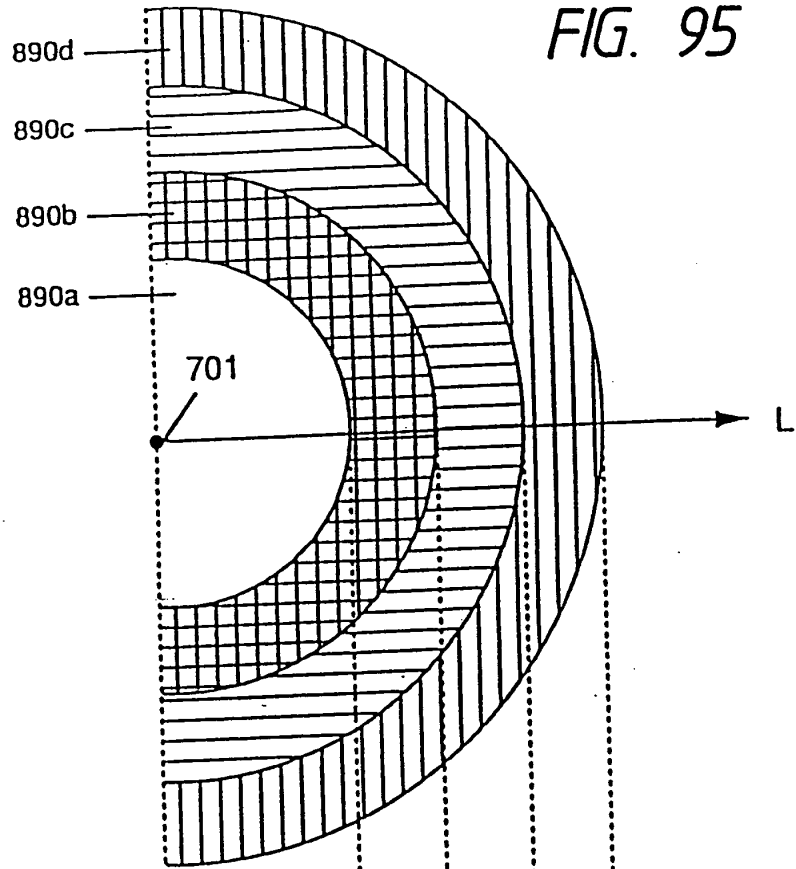


FIG. 96

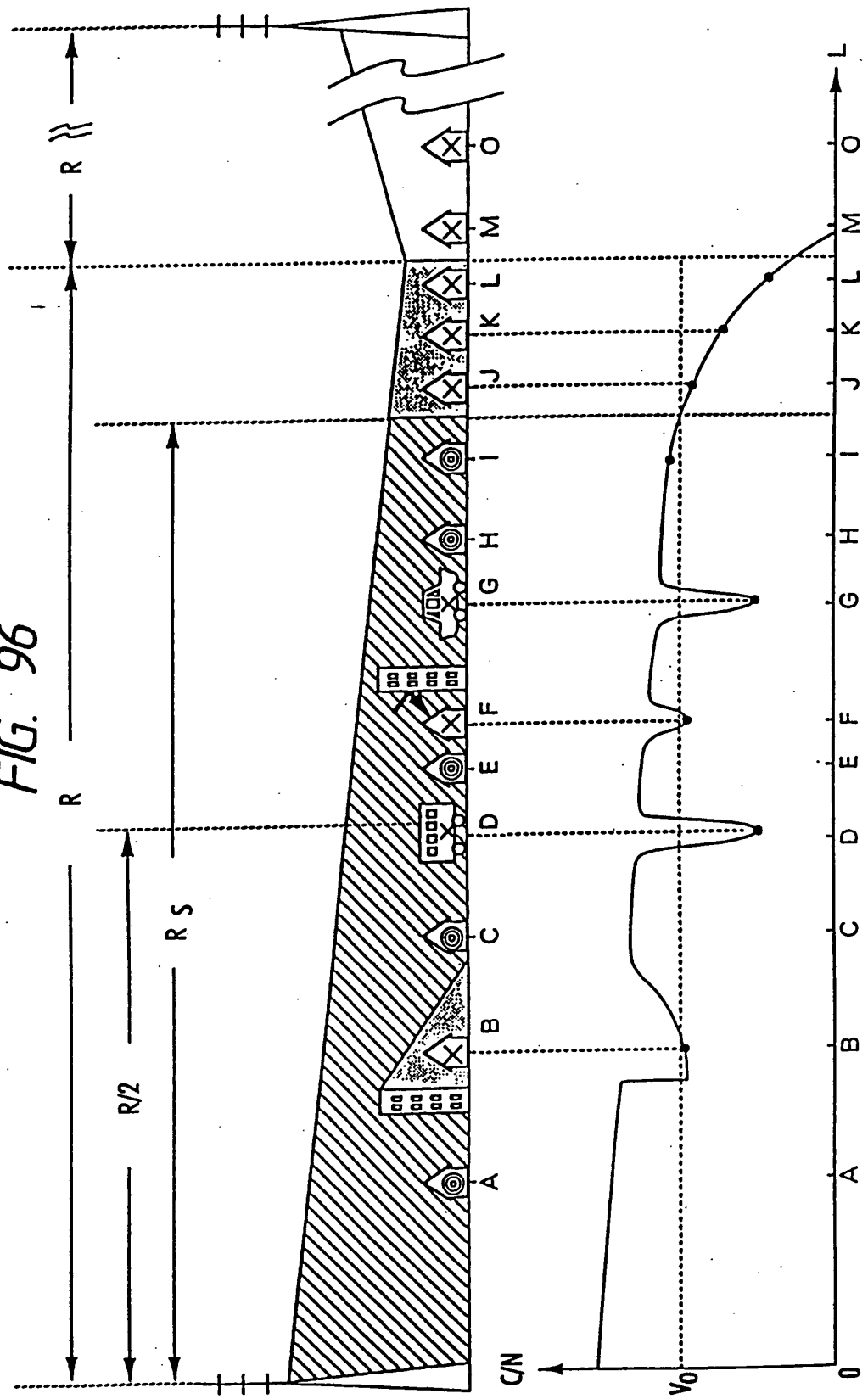


FIG. 97

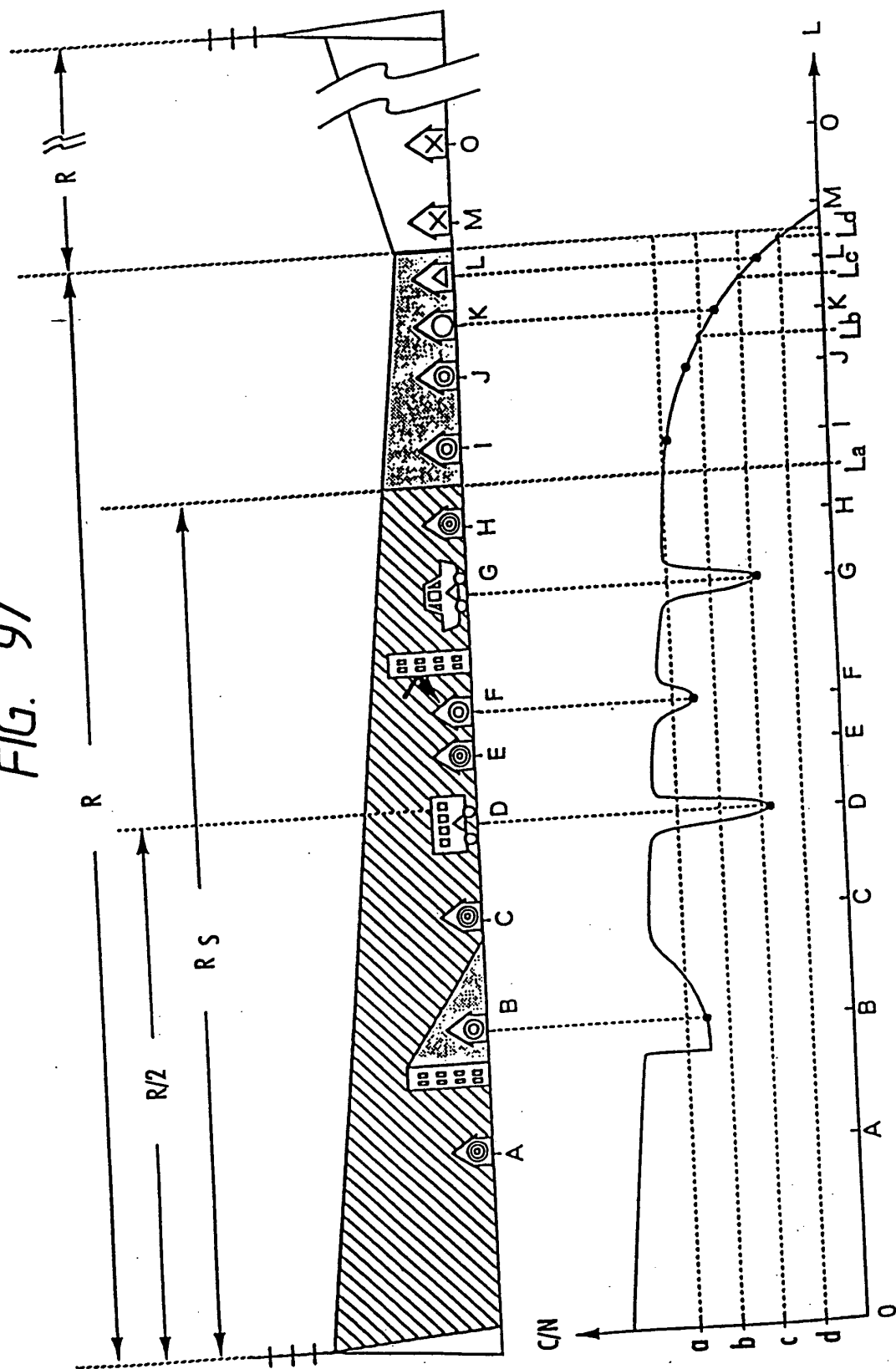


FIG. 98

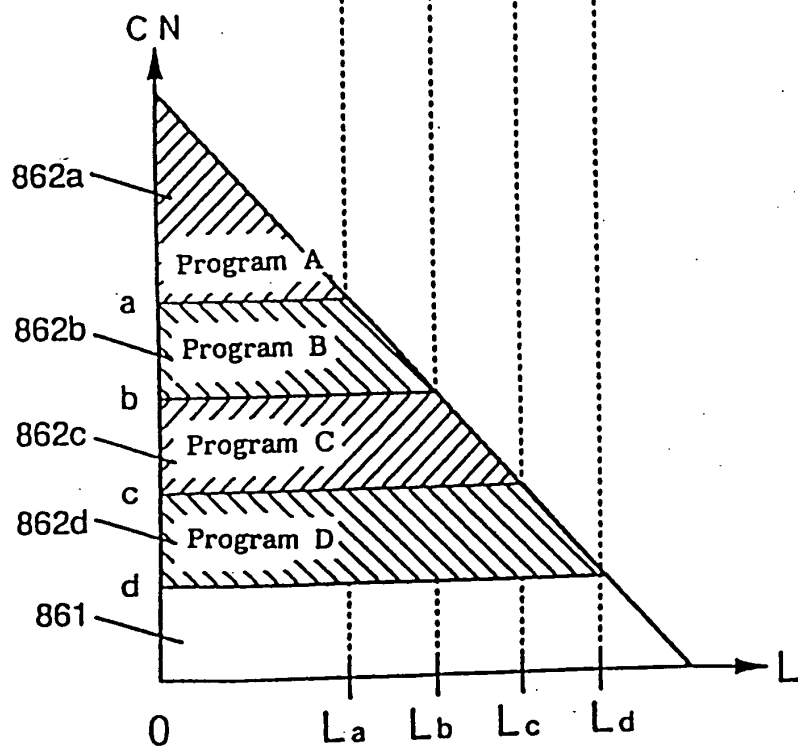
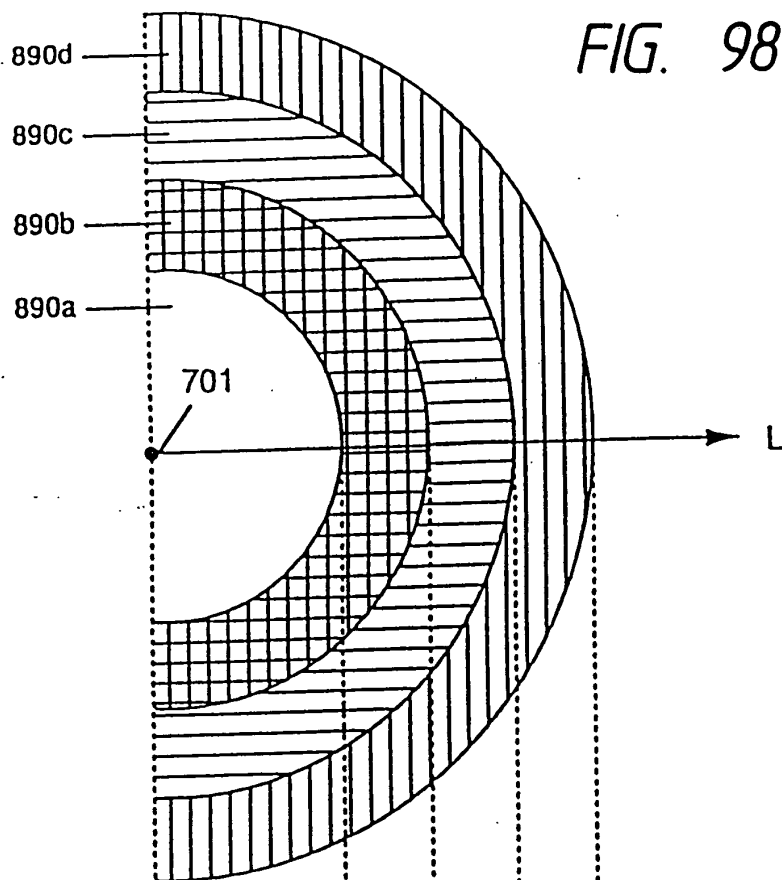


FIG. 99

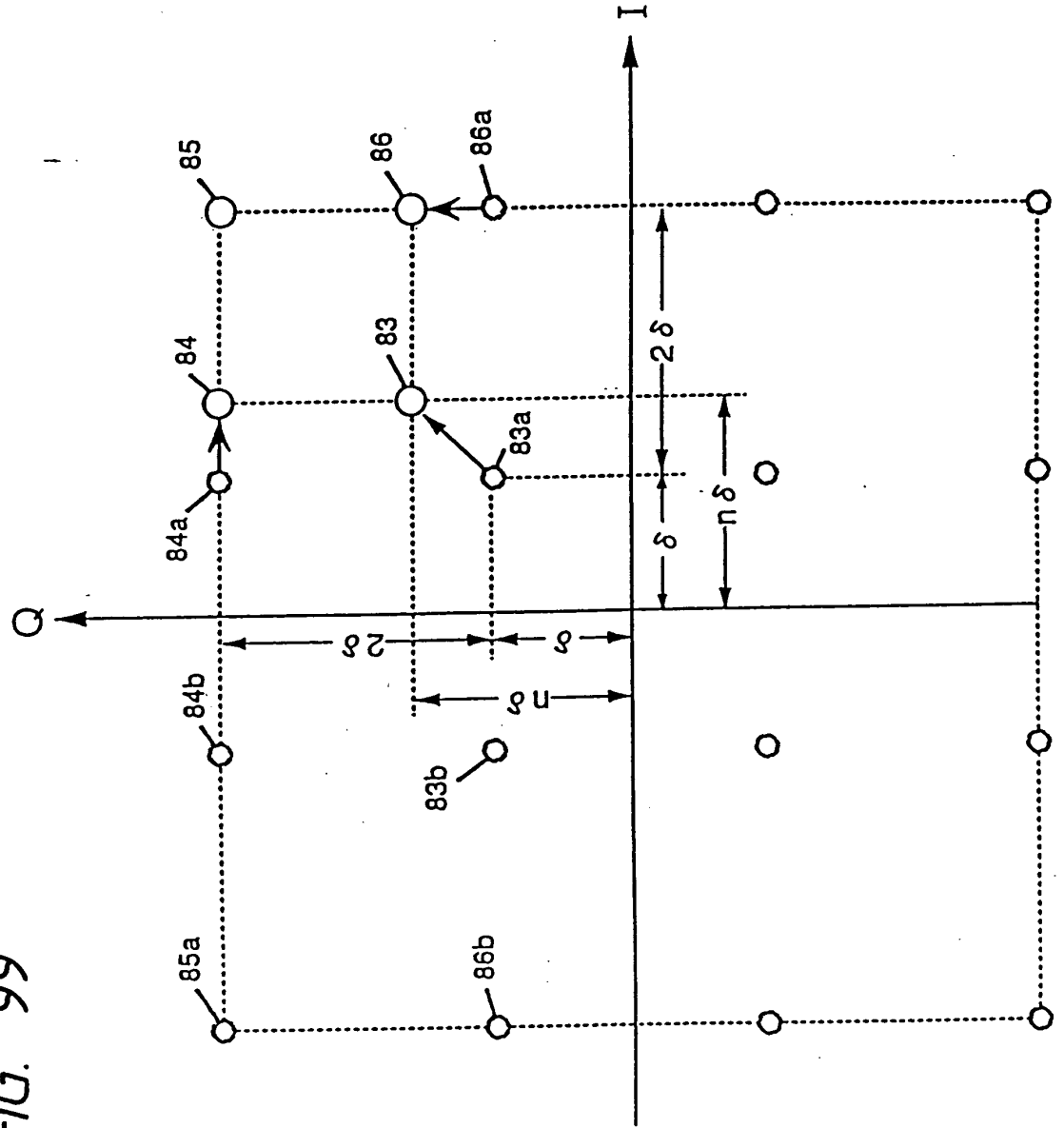


FIG. 100

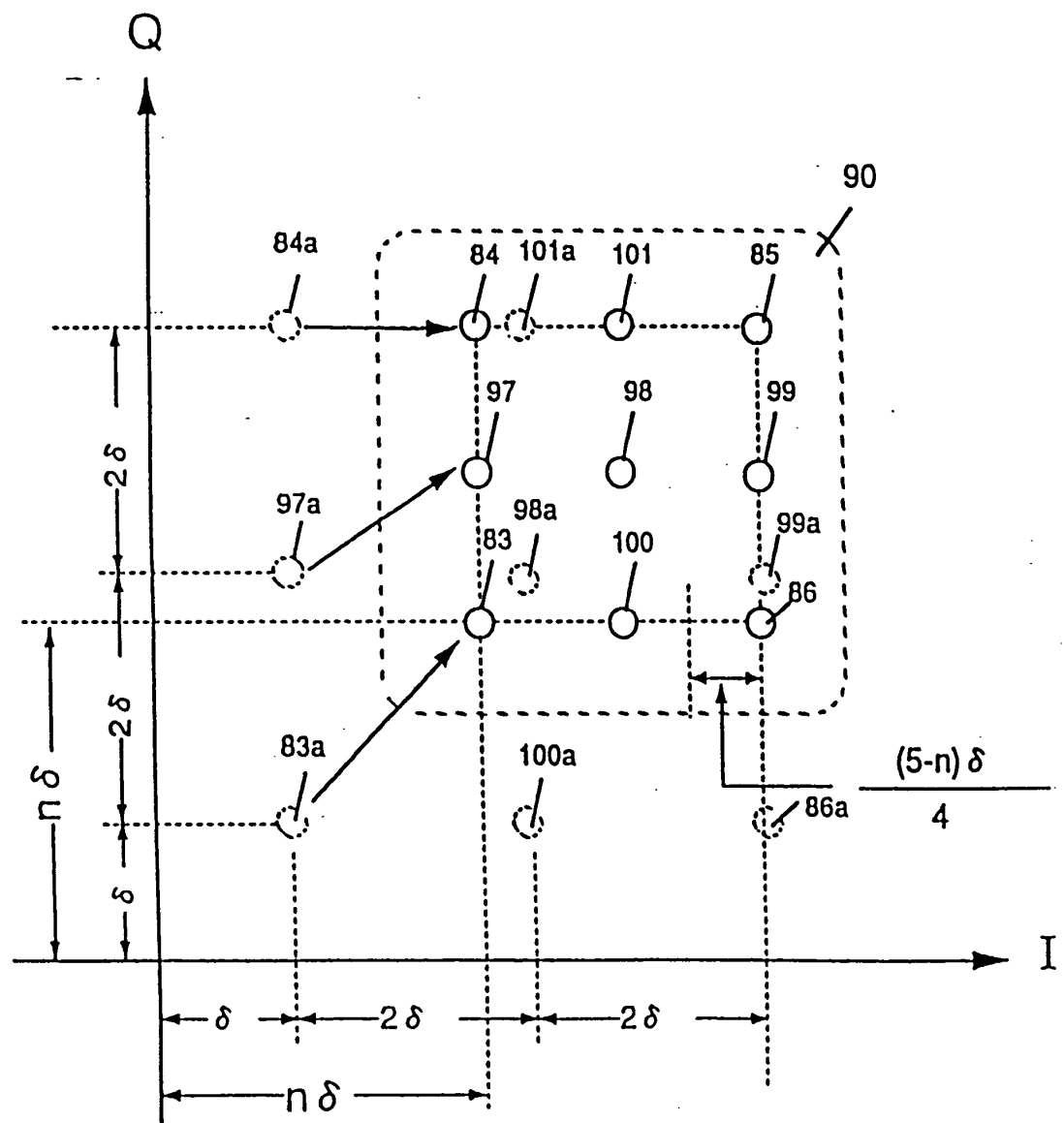


FIG. 101

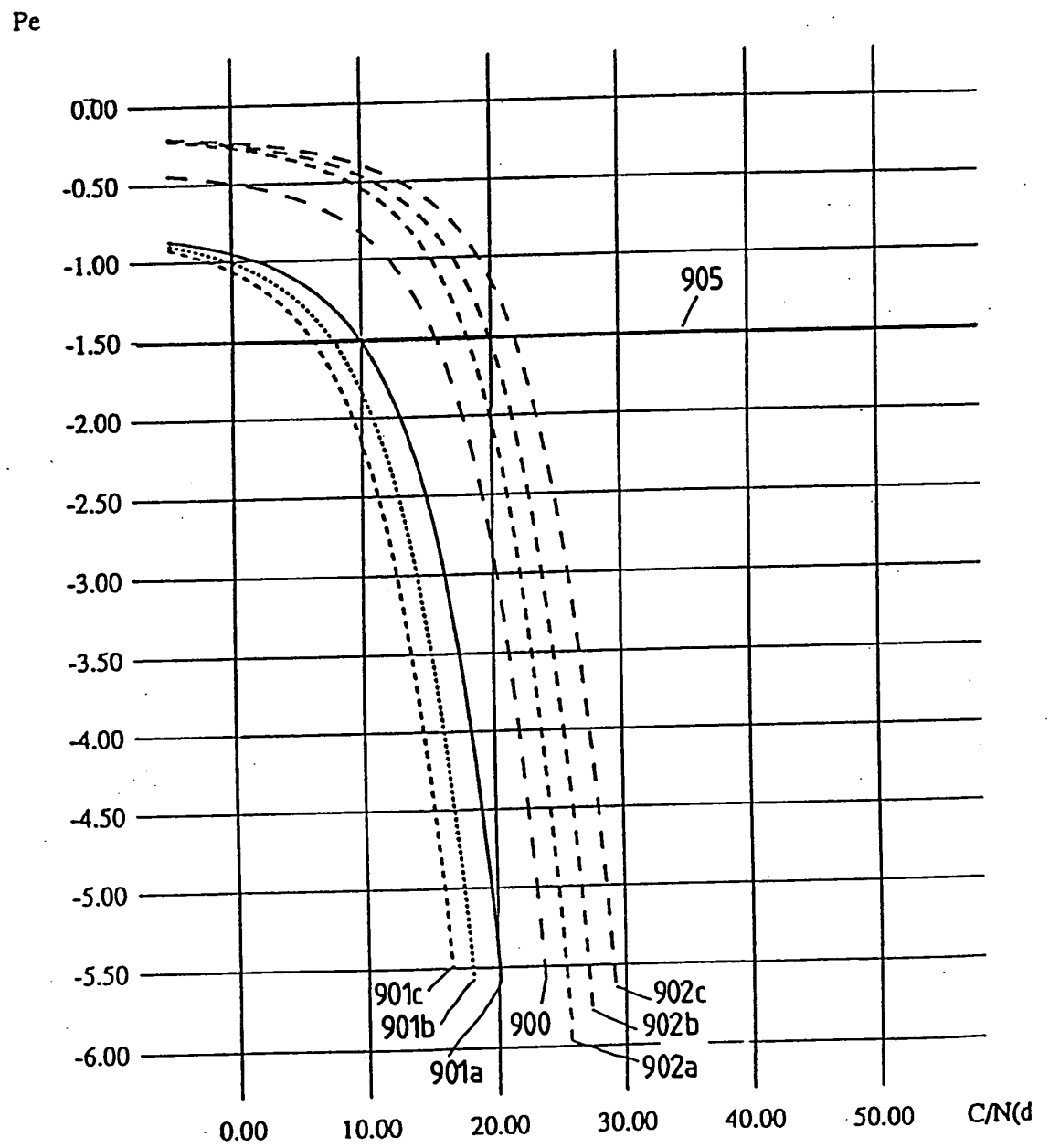


FIG. 102

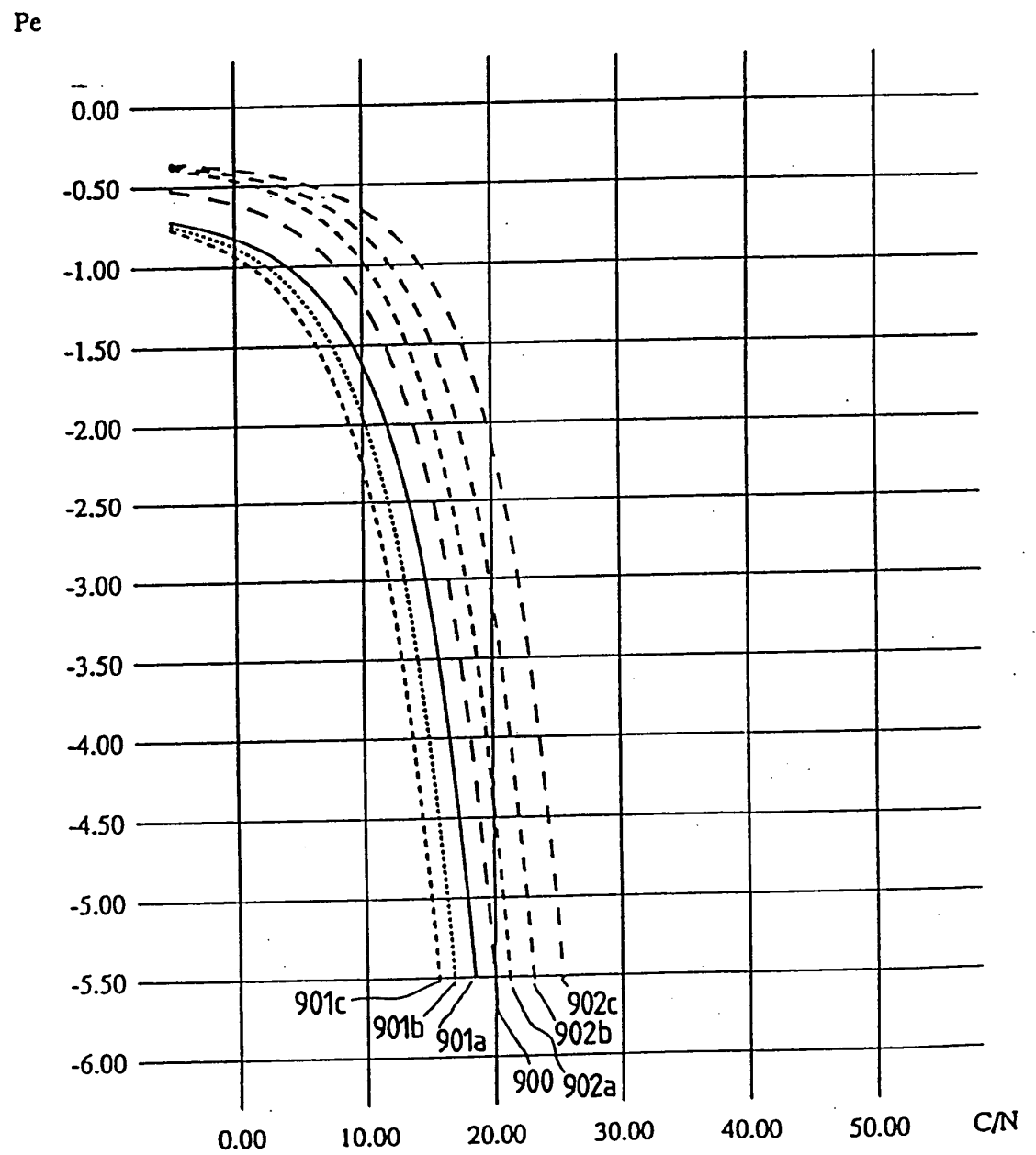


FIG. 103

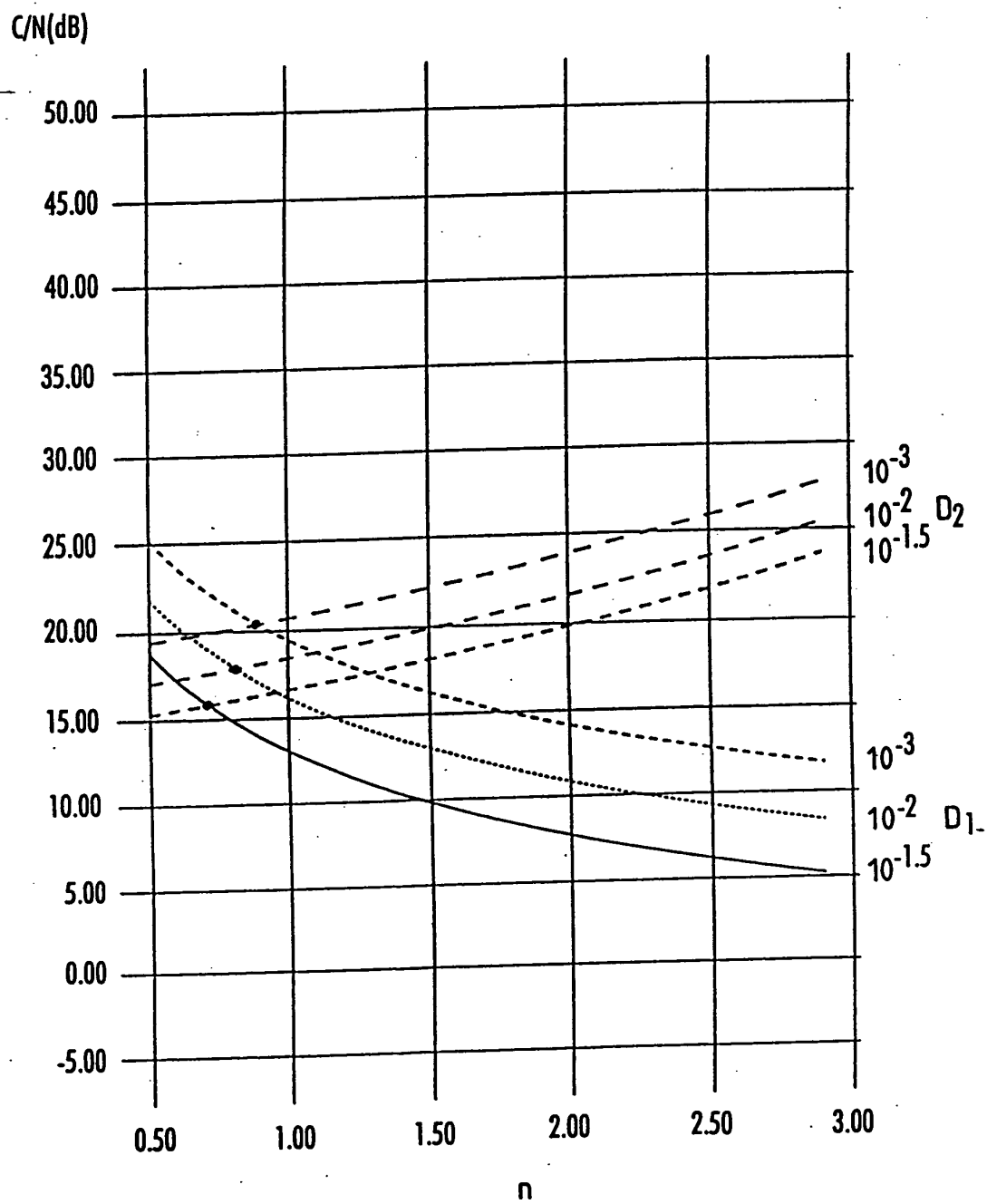


FIG. 104

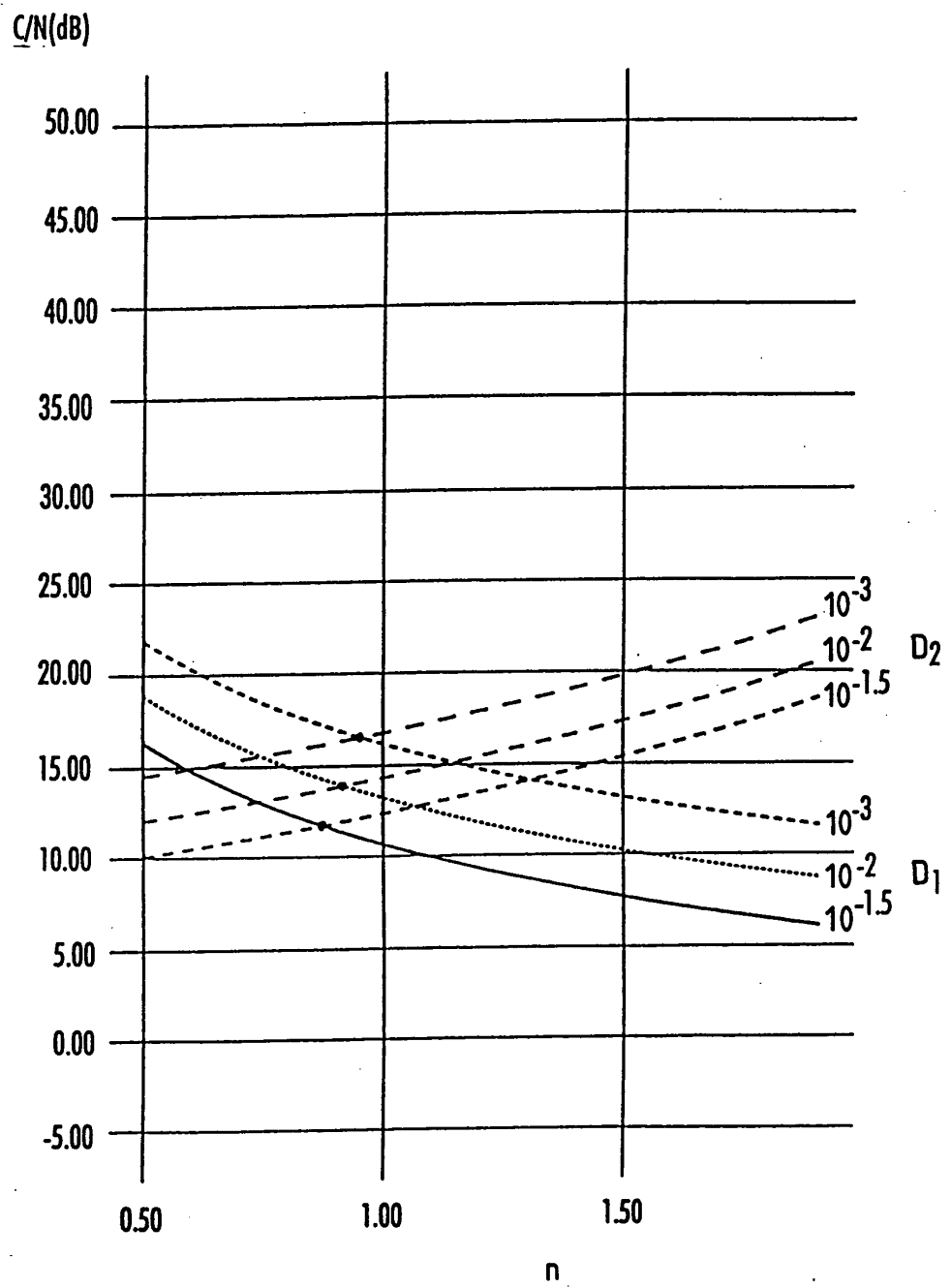


FIG. 105

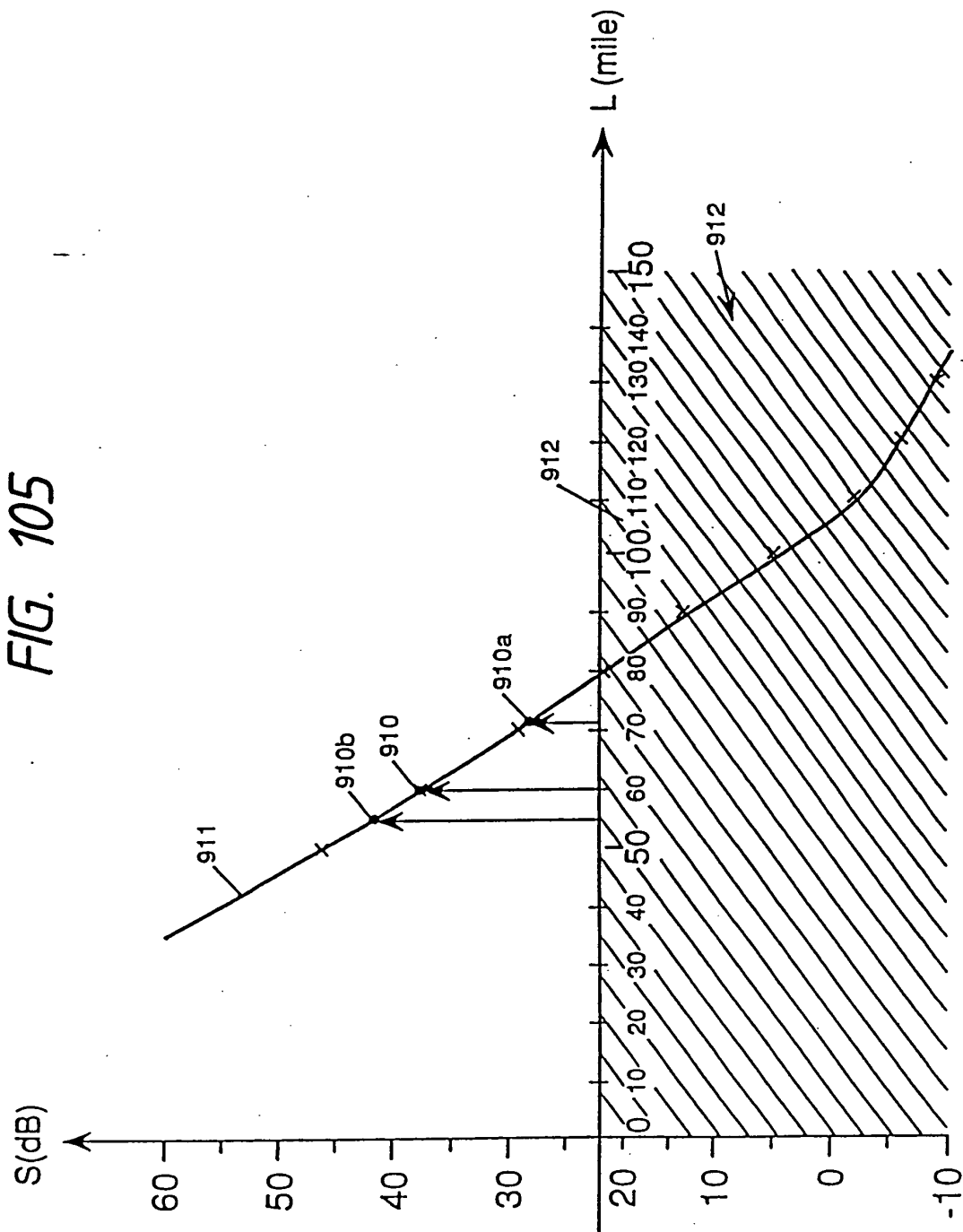


FIG. 106

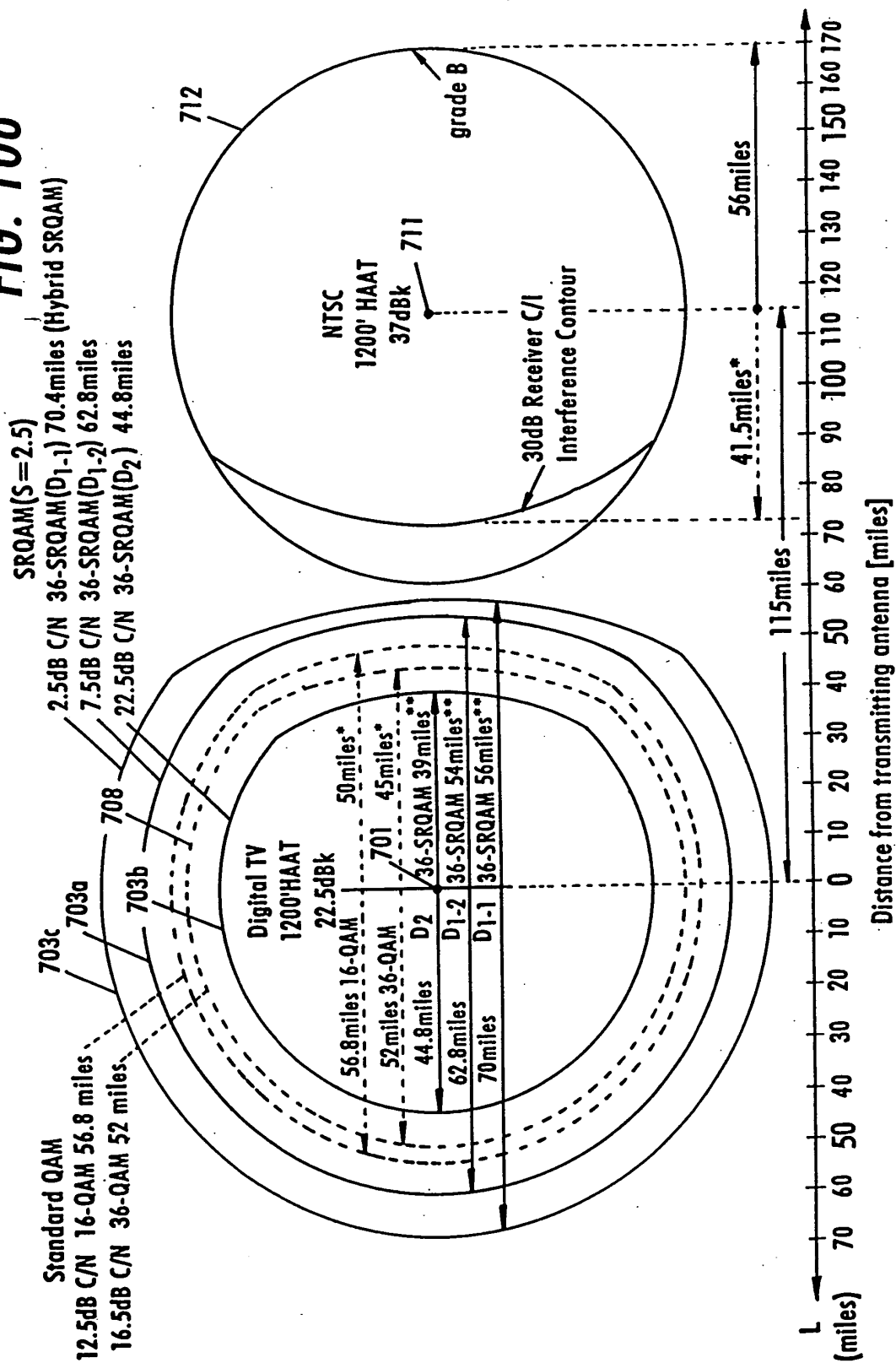


FIG. 107

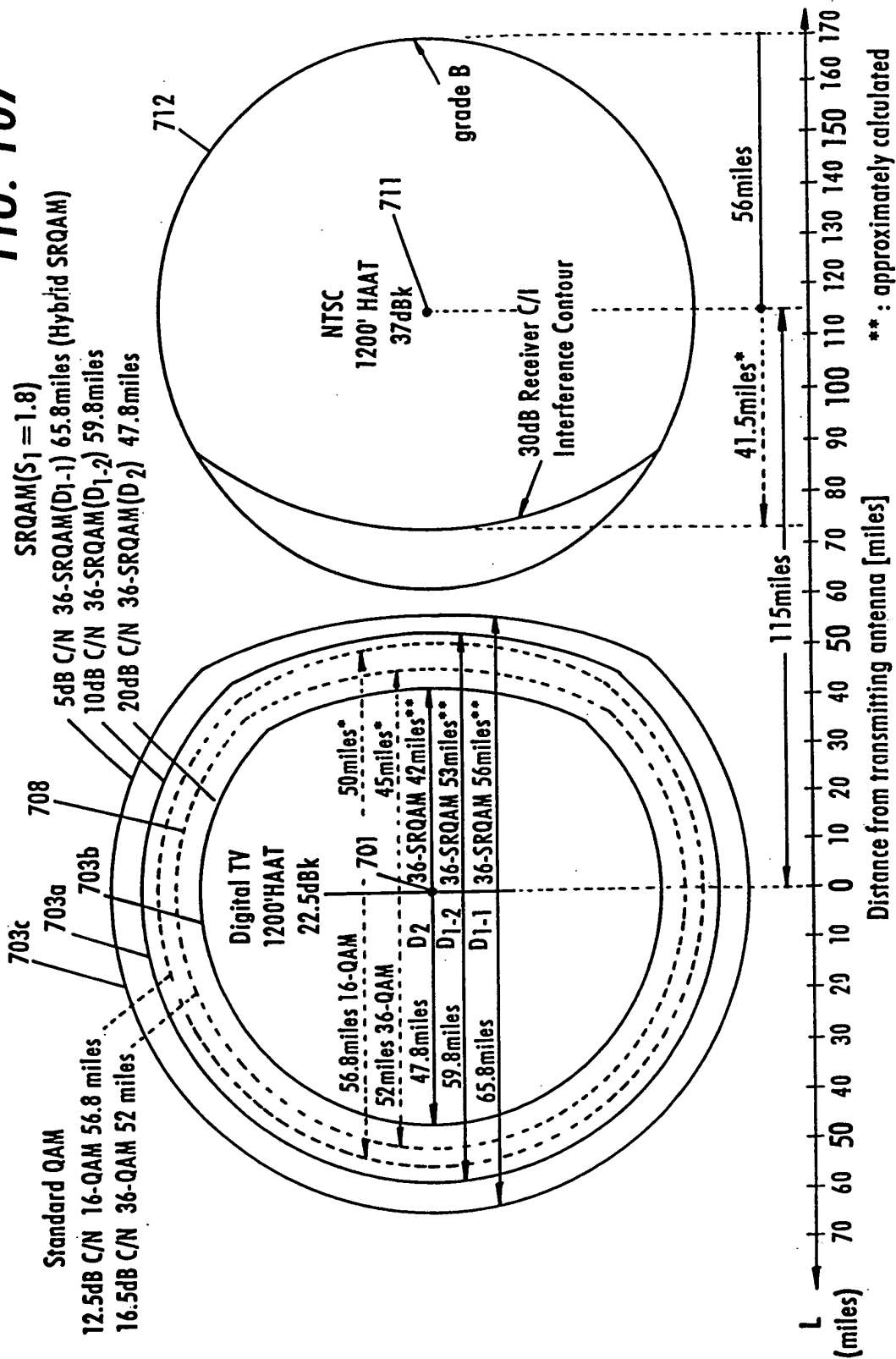


FIG. 108(A)

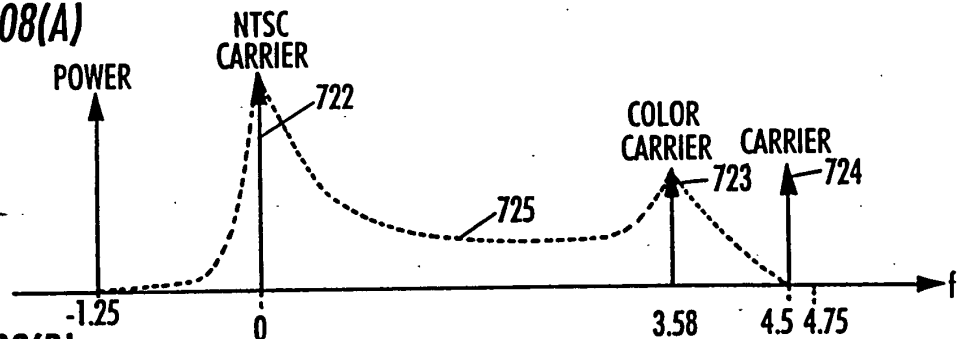


FIG. 108(B)

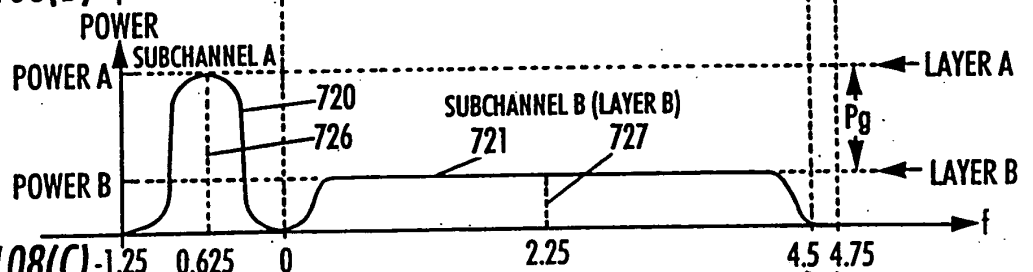


FIG. 108(C)

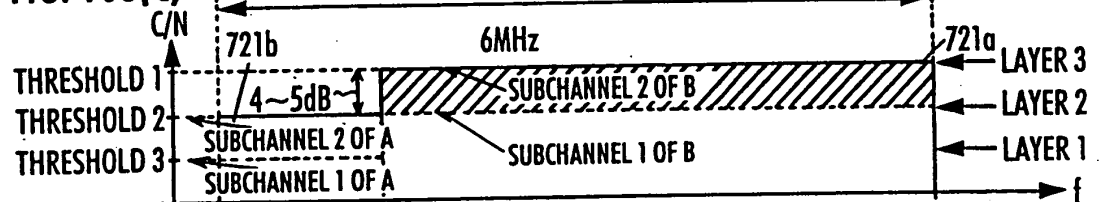


FIG. 108(D)

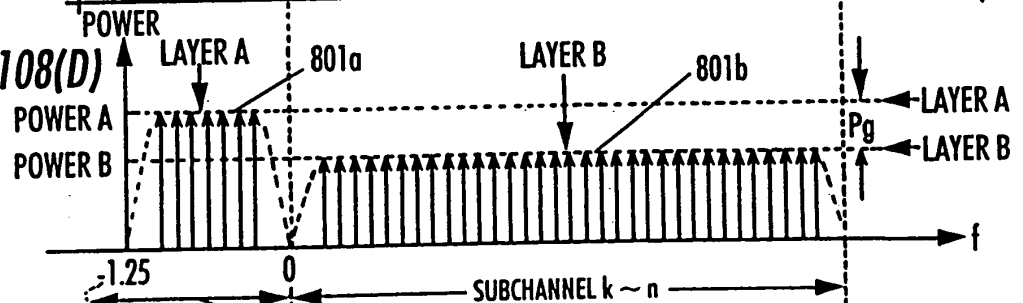


FIG. 108(E)

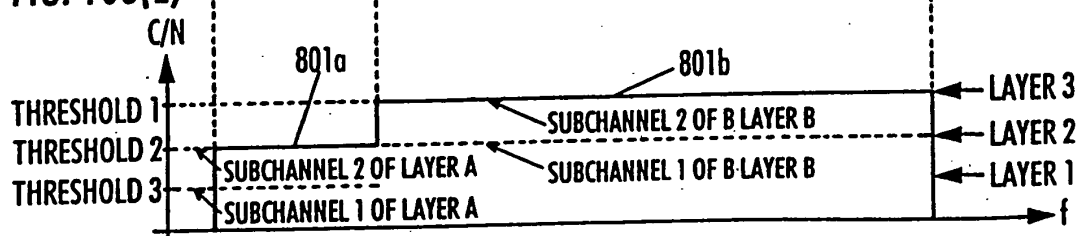


FIG. 109

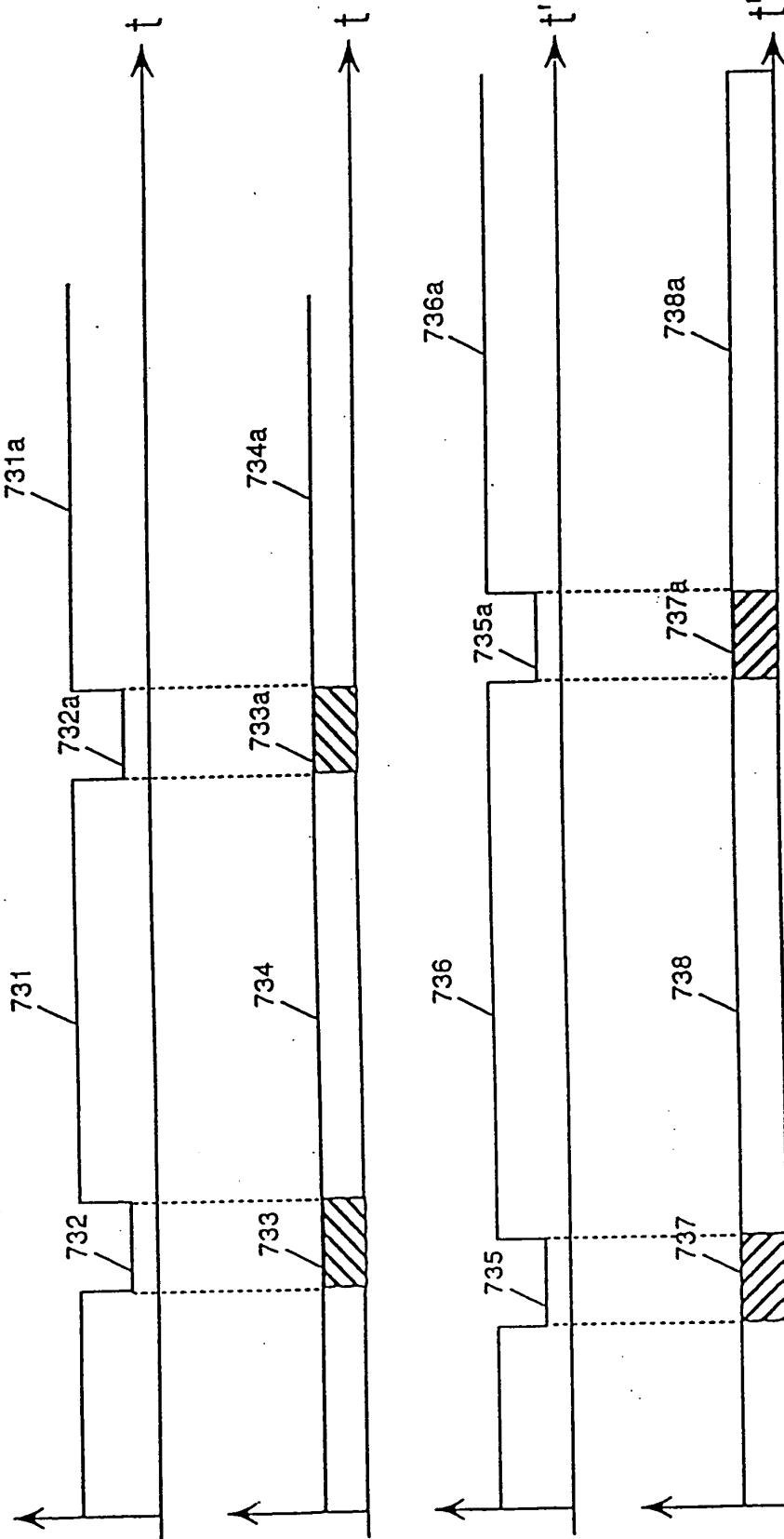


FIG. 110

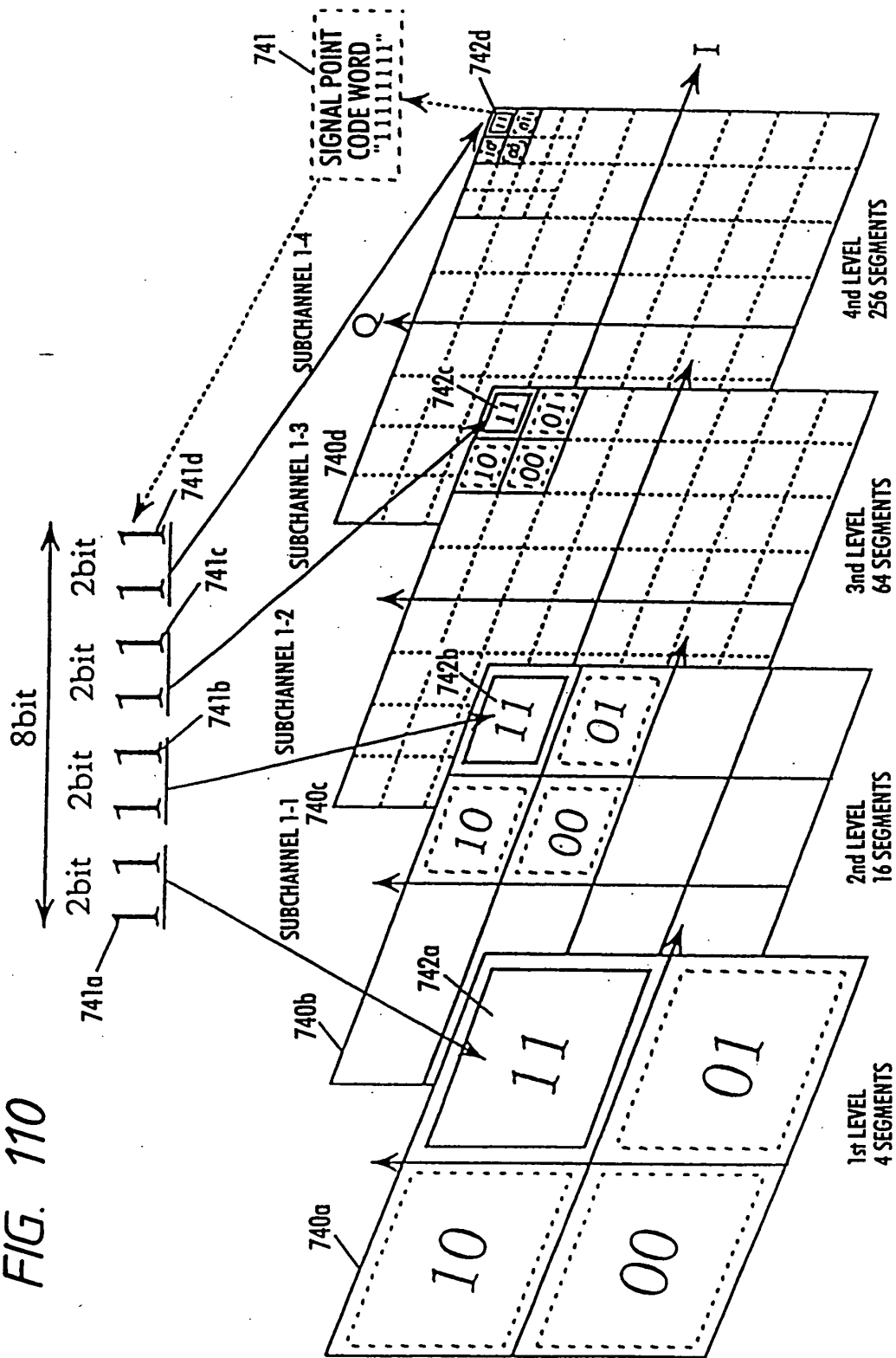
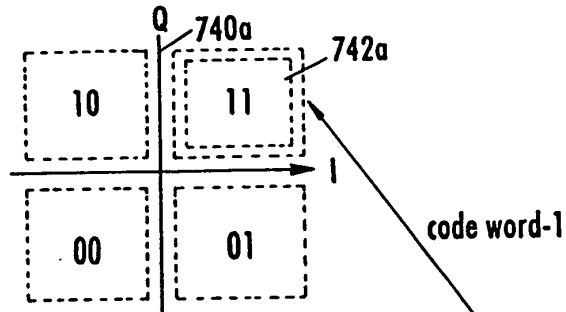
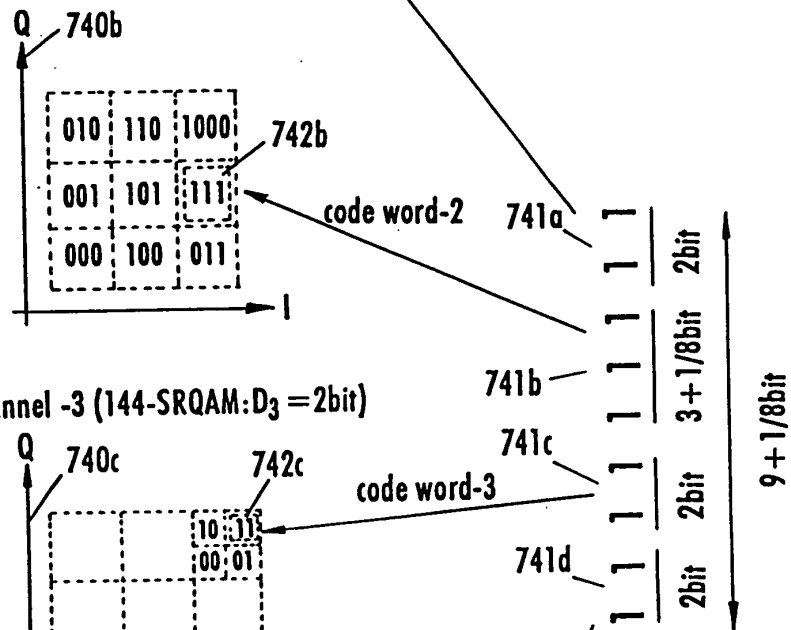


FIG. 111

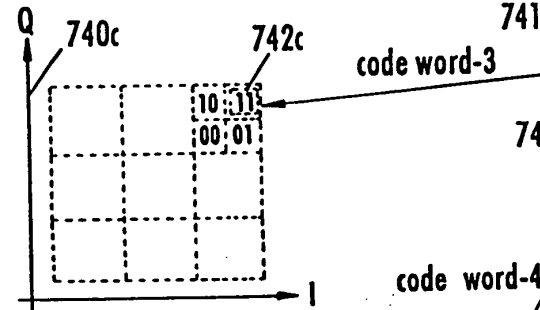
Subchannel -1 (SRQAM: $D_1 = 2\text{bit}$)



Subchannel -2 (36-SRQAM: $D_2 = 3\text{bit} + 1/8\text{bit}$)



Subchannel -3 (144-SRQAM: $D_3 = 2\text{bit}$)



Subchannel -4 (576-SRQAM: $D_4 = 2\text{bit}$)

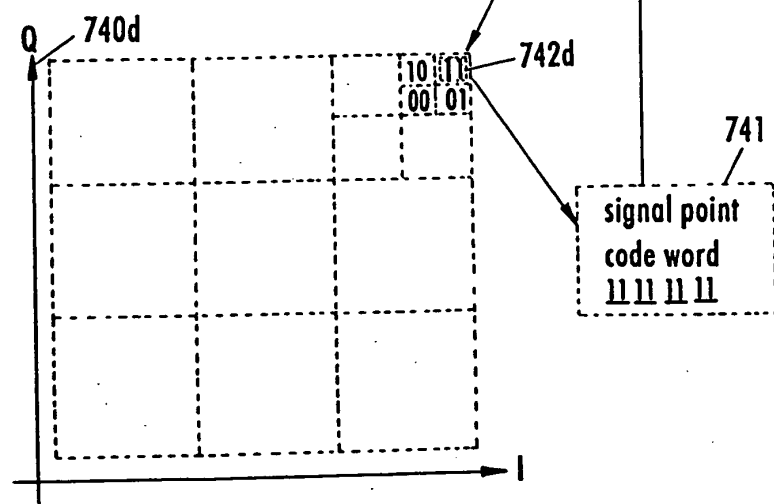
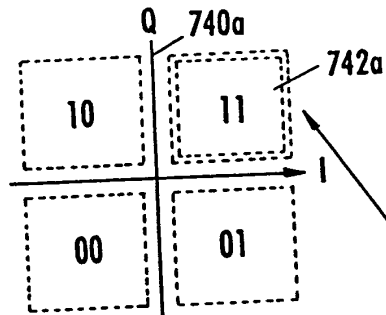
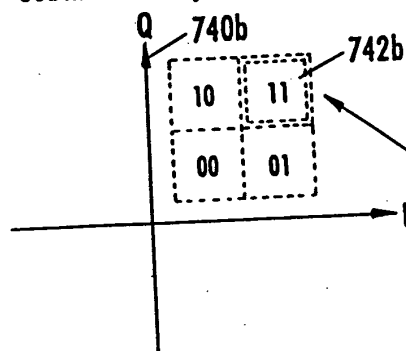


FIG. 112

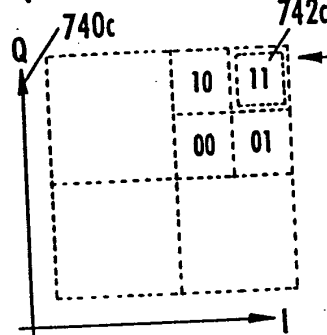
Subchannel -1 (SRQAM: $D_1 = 2\text{bit}$)



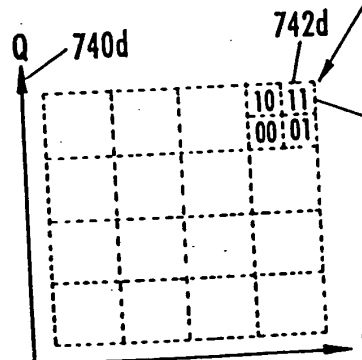
Subchannel -2 (16-SRQAM: $D_2 = 2\text{bit}$)



Subchannel -3 (64-SRQAM: $D_3 = 2\text{bit}$)



Subchannel -4 (256-SRQAM: $D_4 = 2\text{bit}$)



code word-1

code word-2

code word-3

code word-4

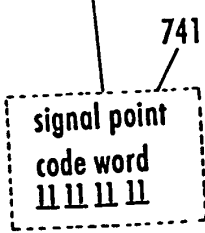
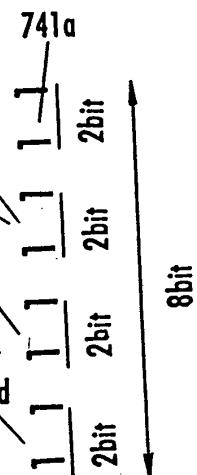


FIG. 113

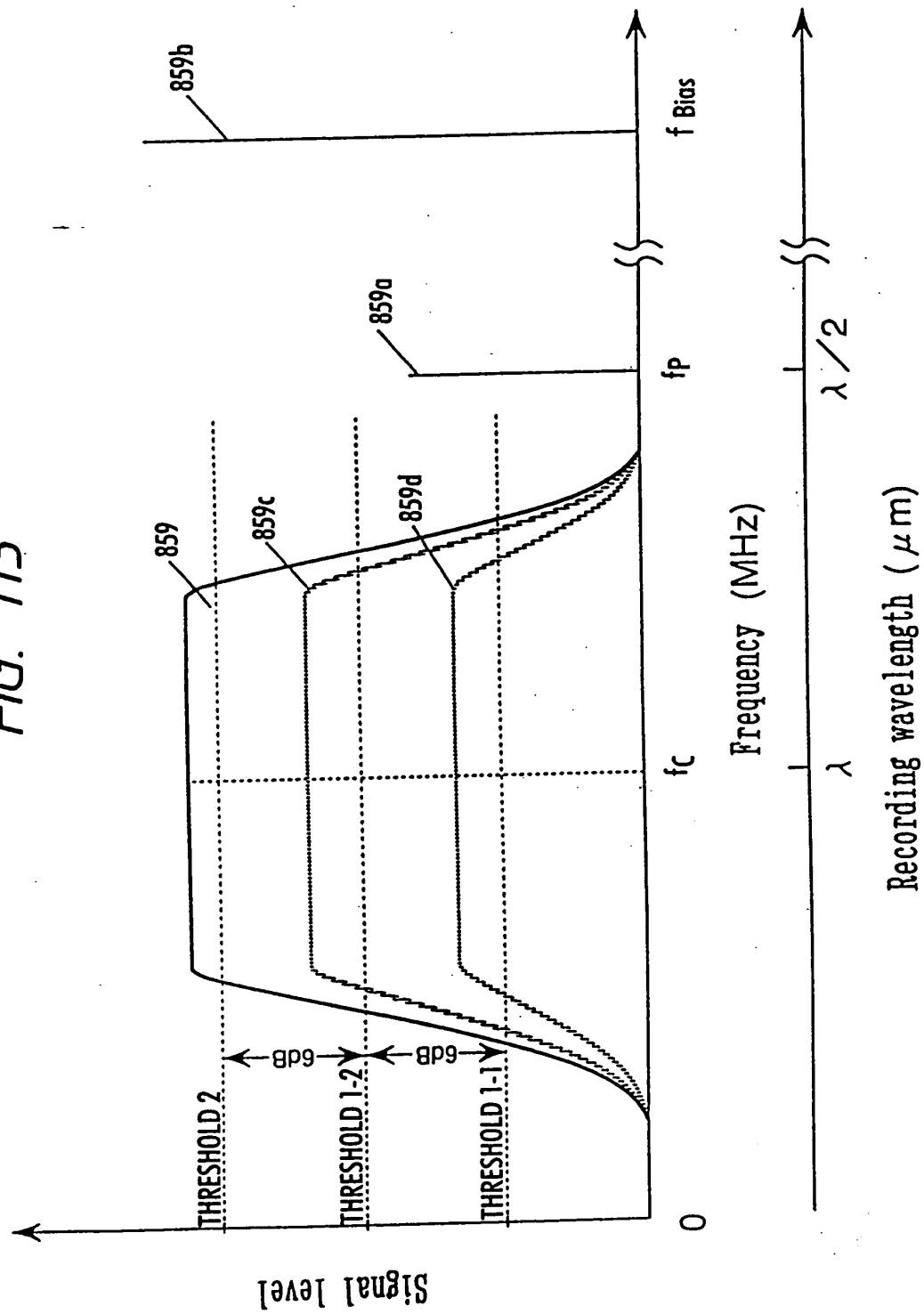


FIG. 114

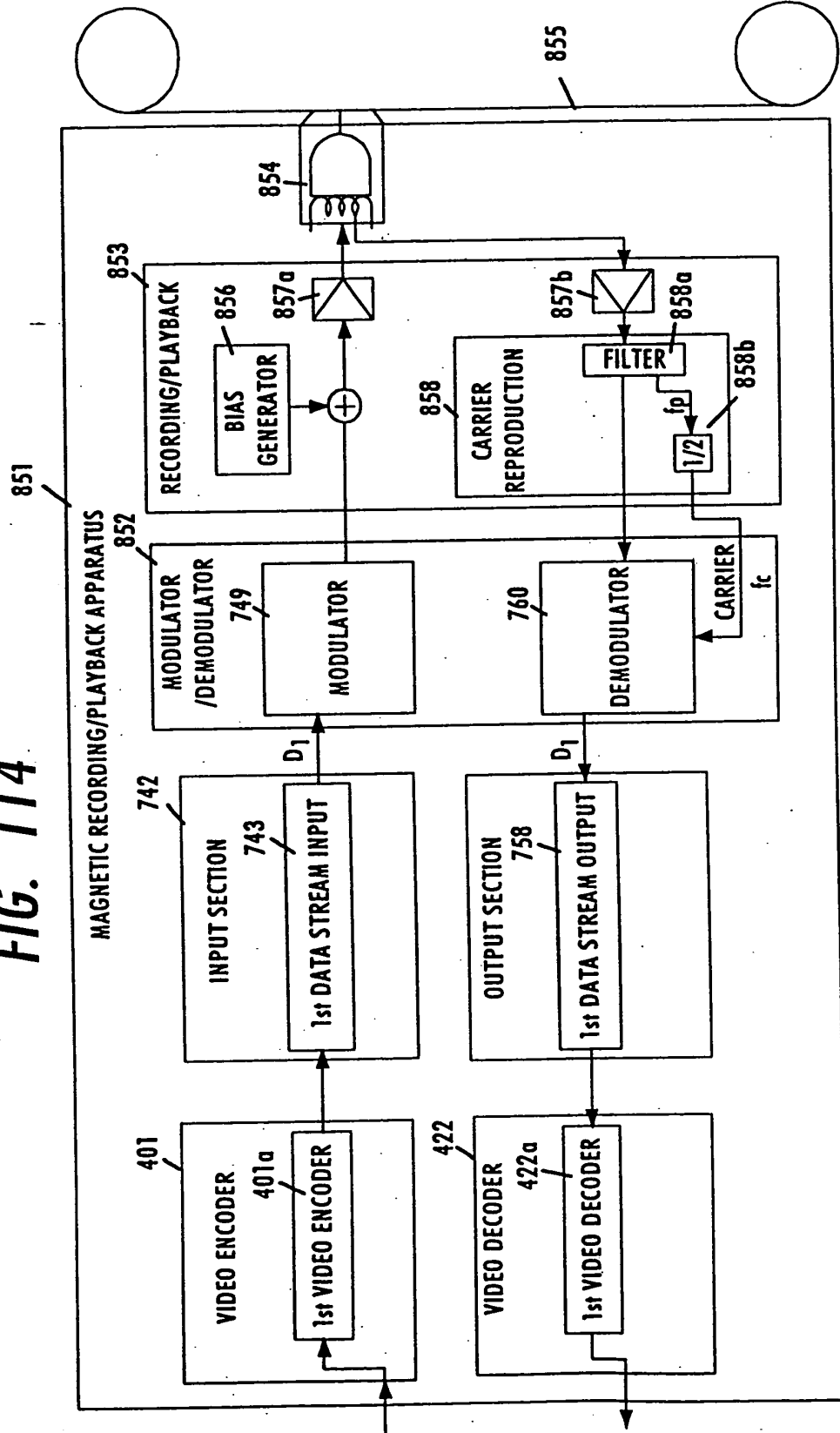


FIG. 115

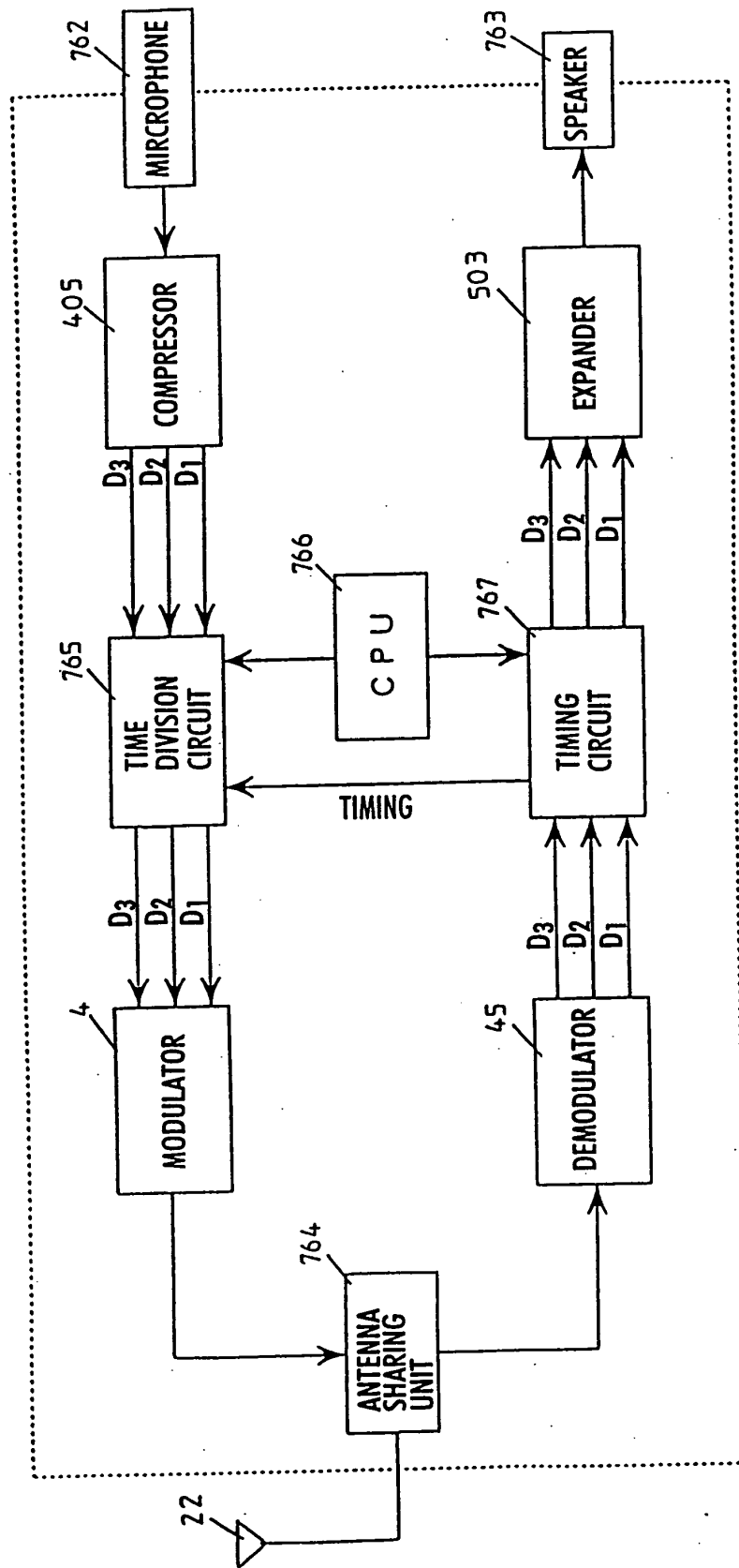


FIG. 116

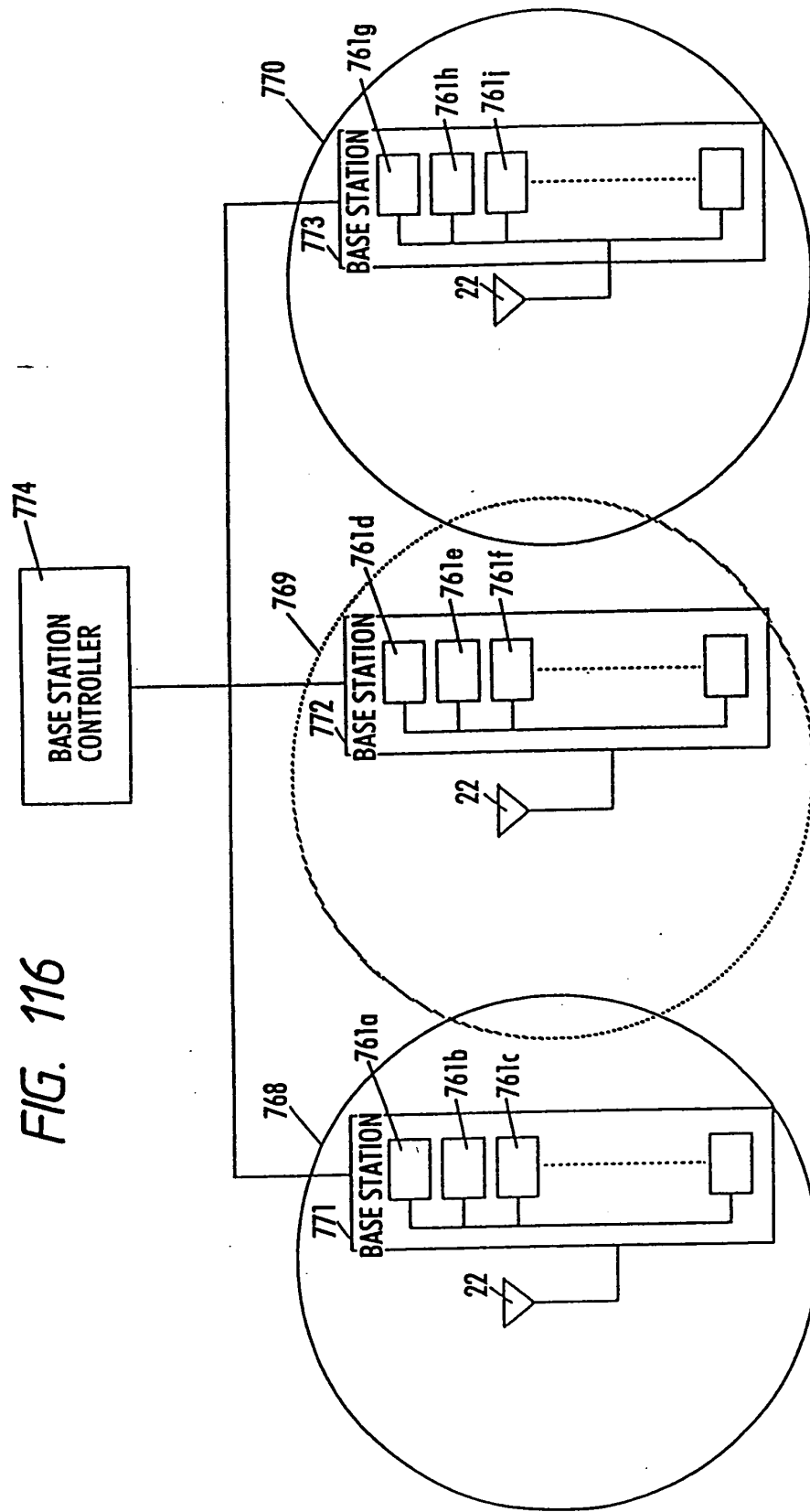


FIG. 117

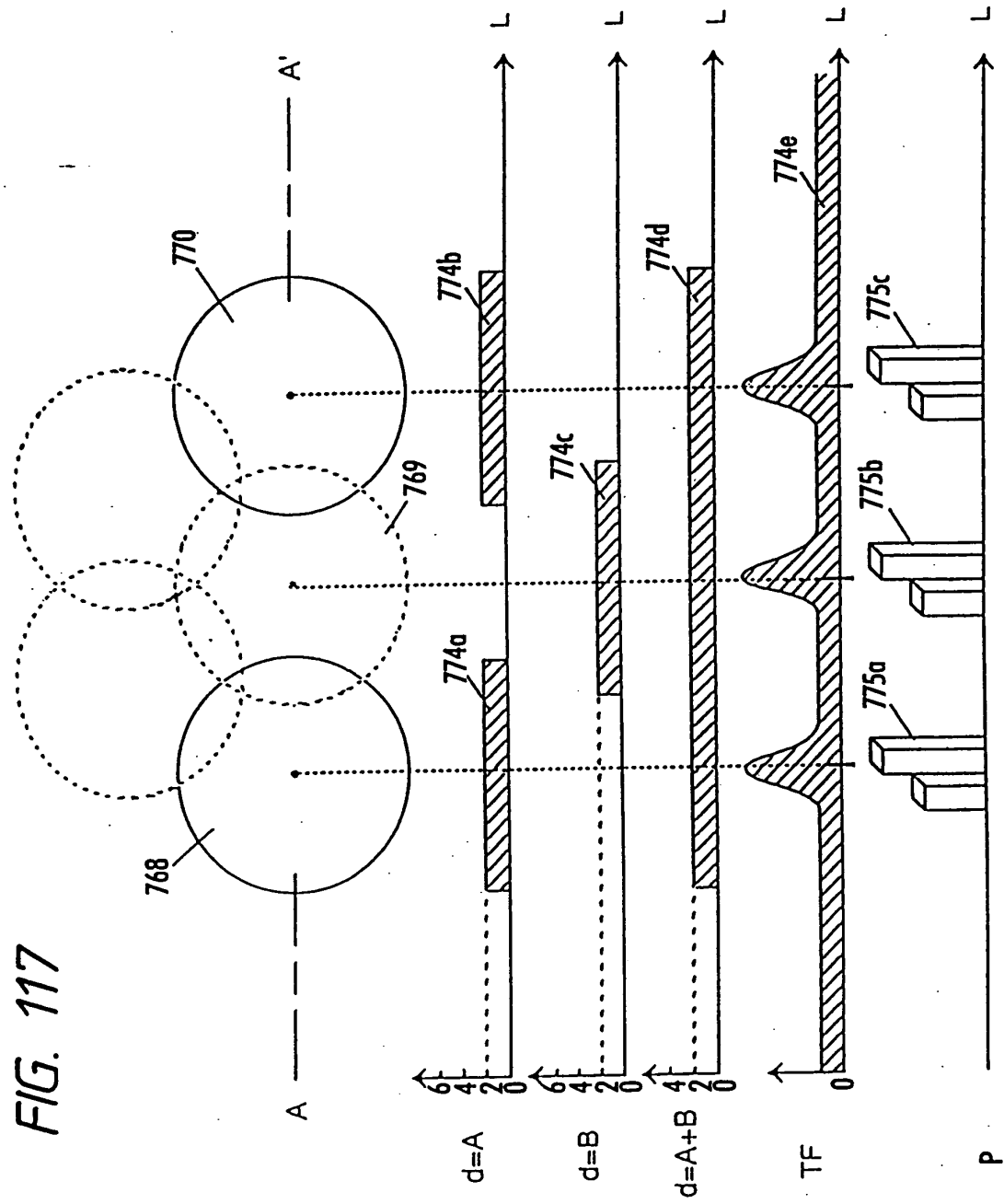


FIG. 118

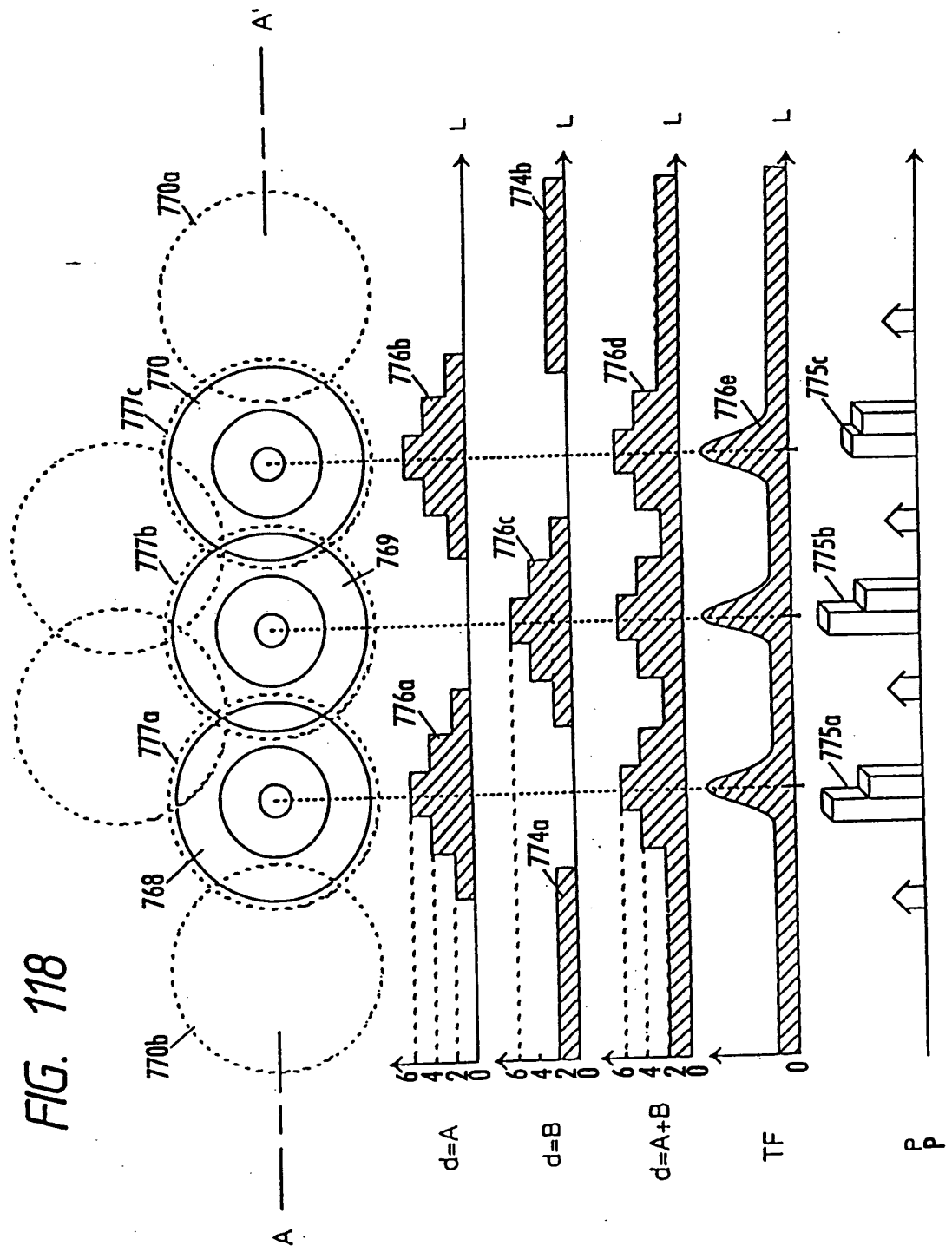


FIG. 119(a)

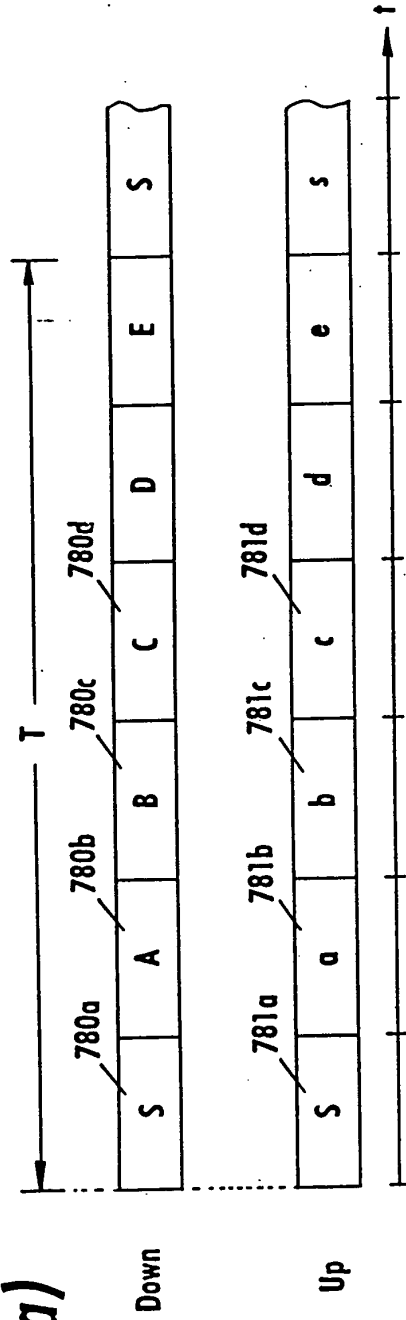


FIG. 119(b)

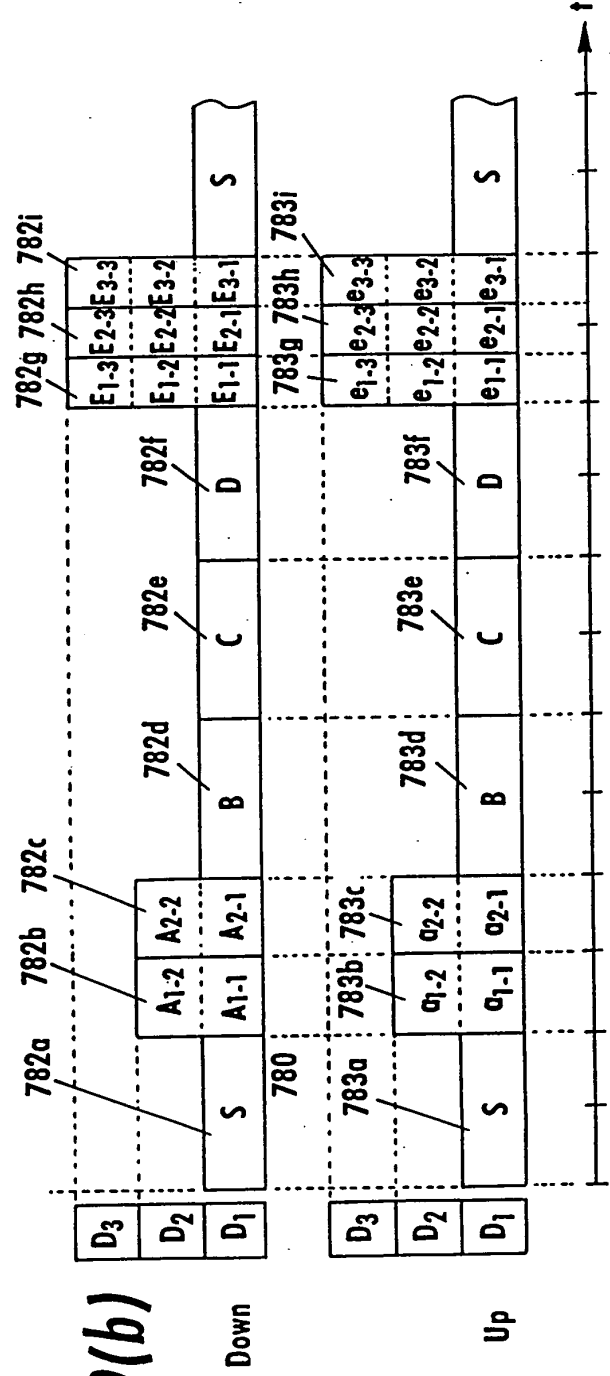


FIG. 120(a)

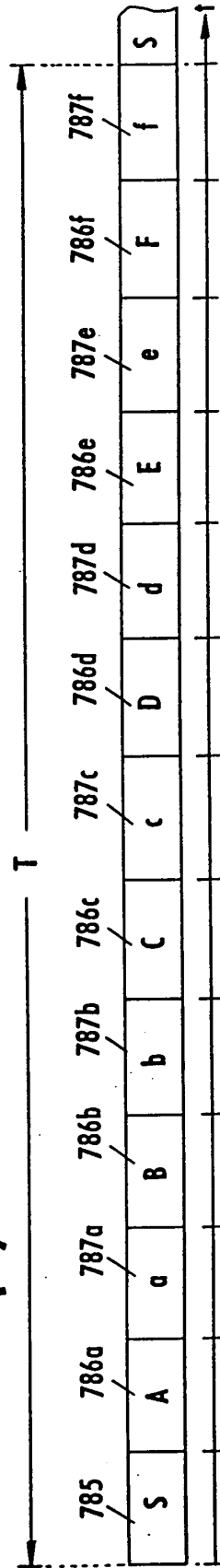


FIG. 120(b)

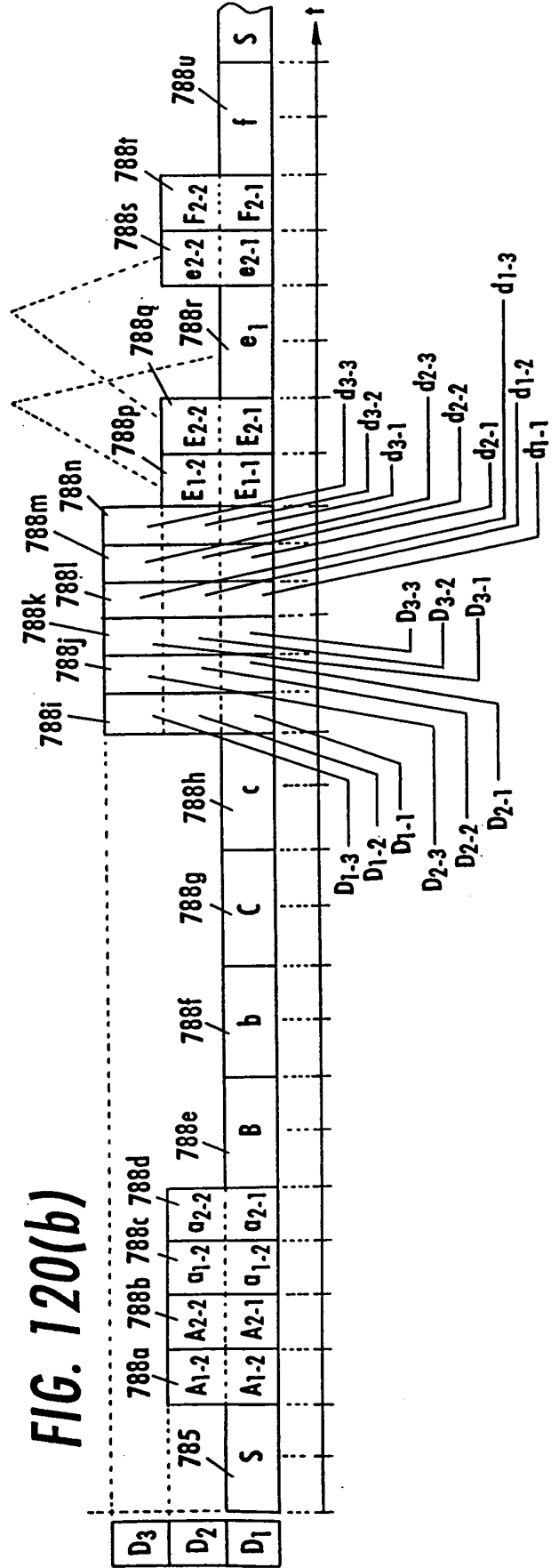


FIG. 121

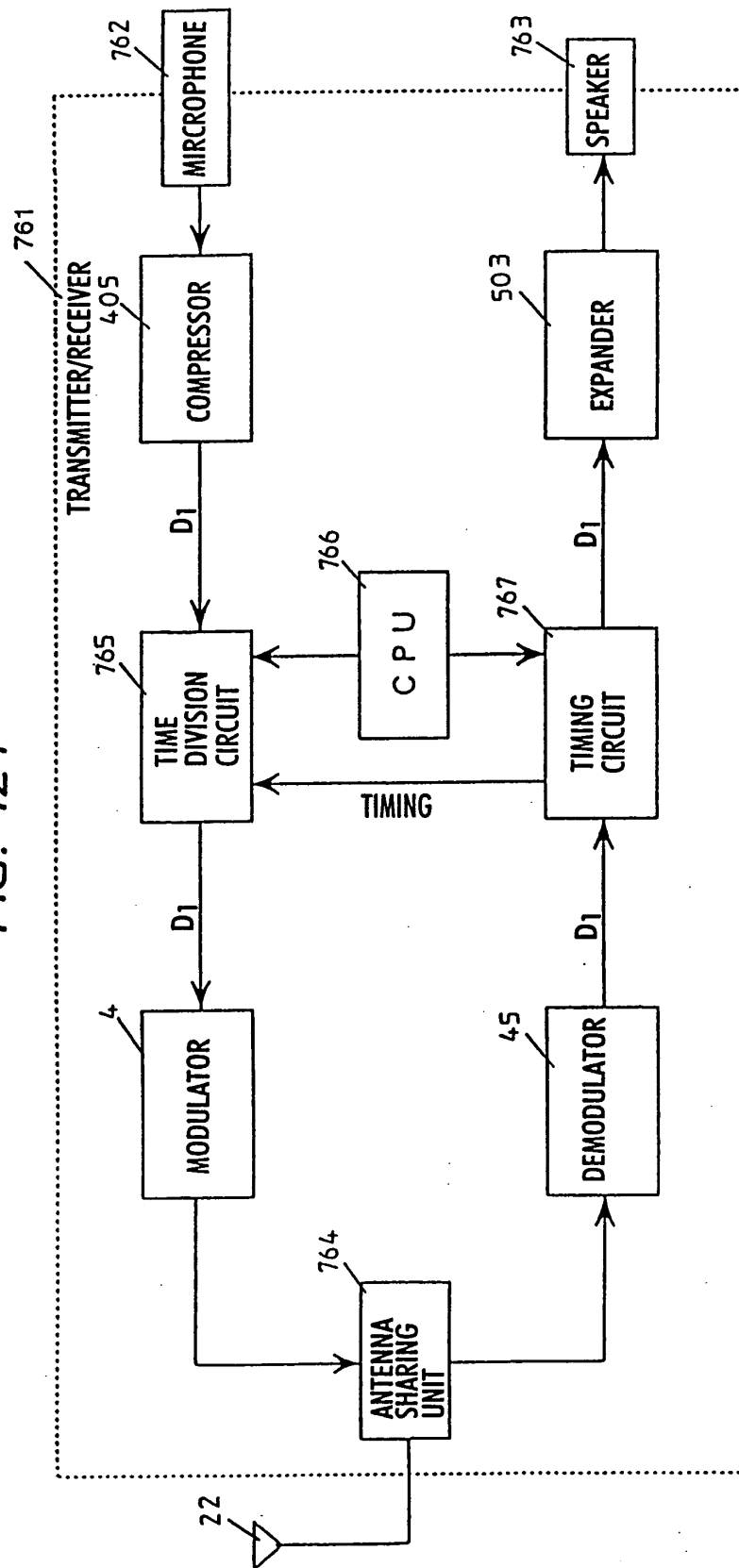


FIG. 122

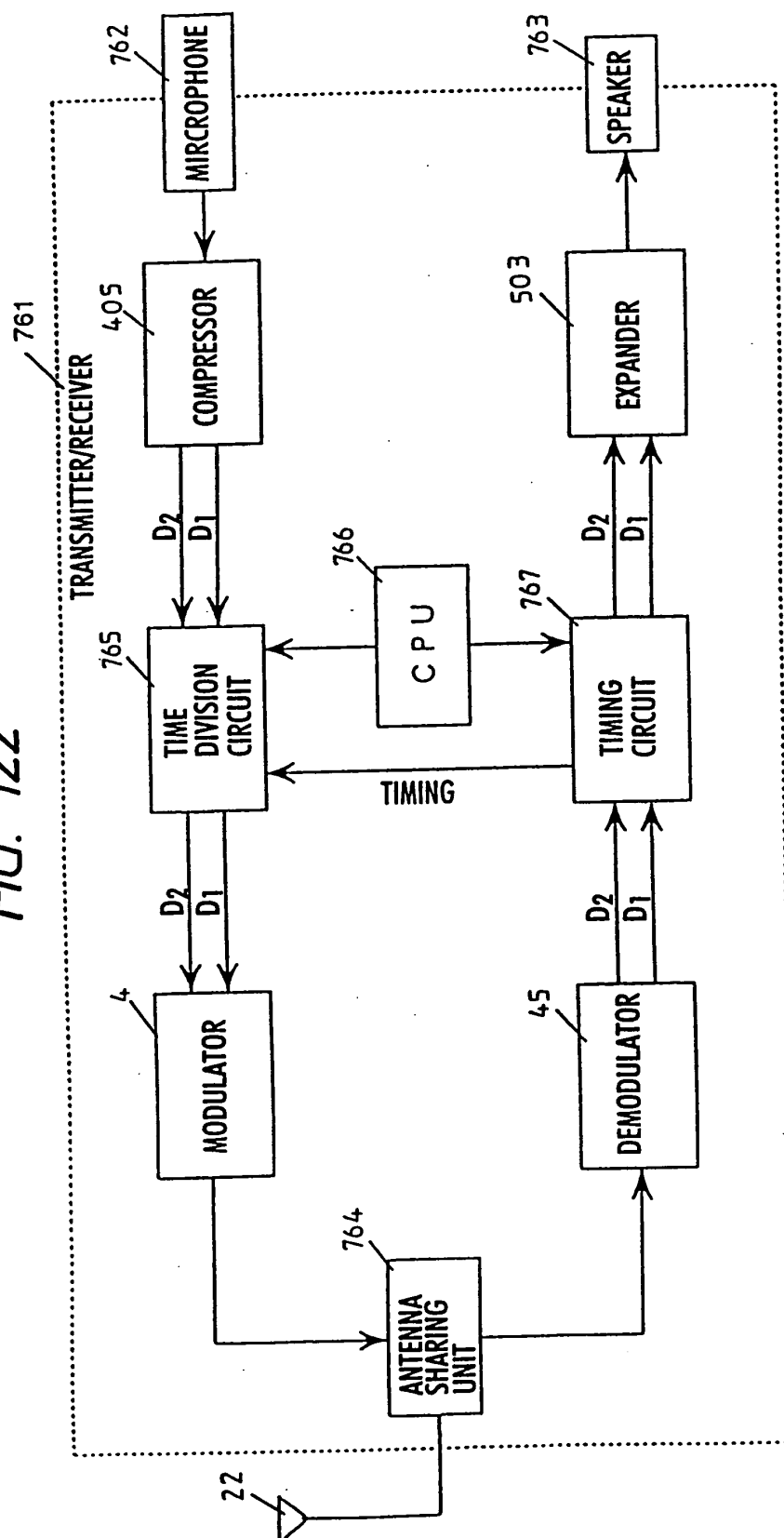


FIG. 123

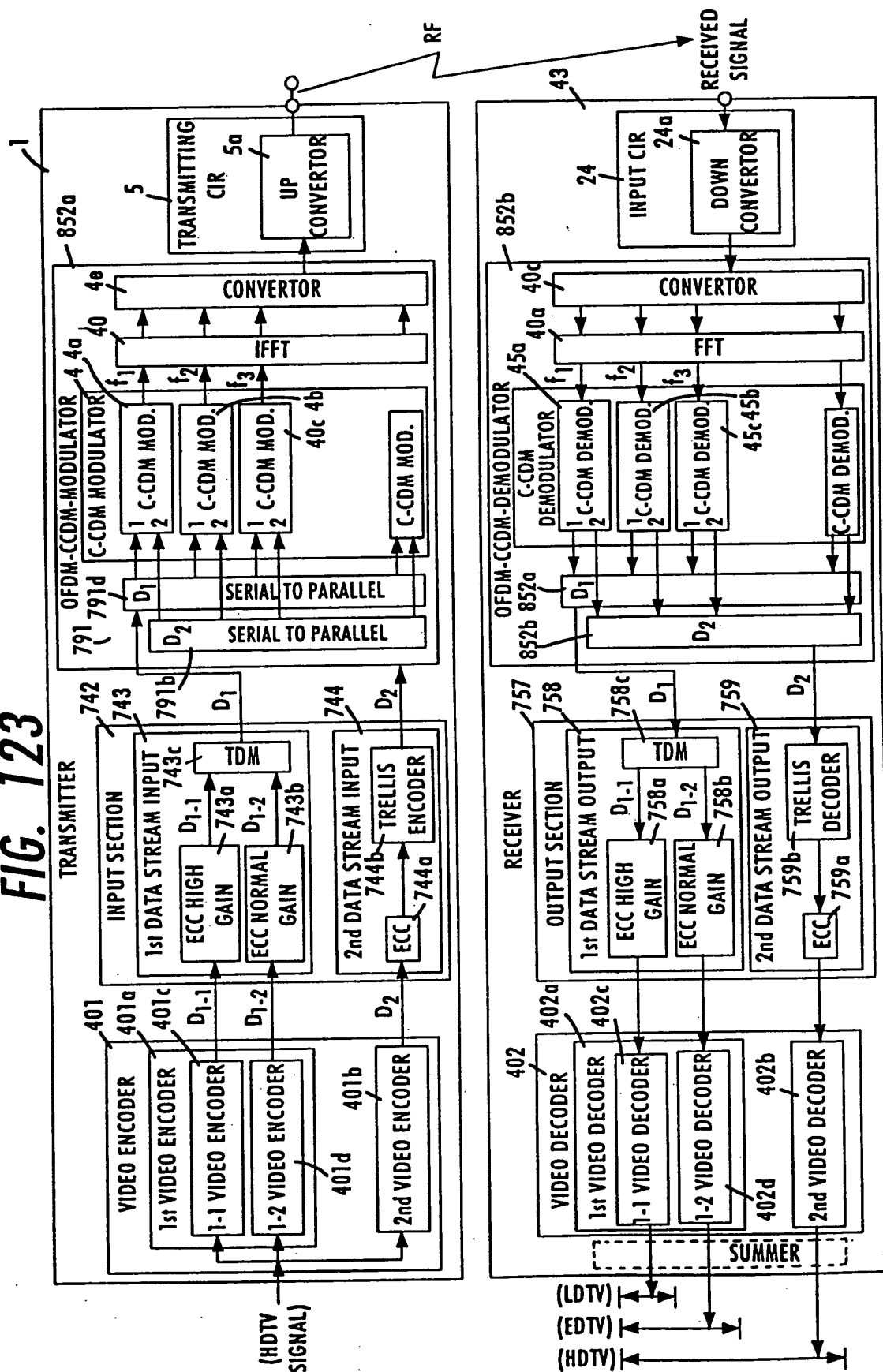


FIG. 124

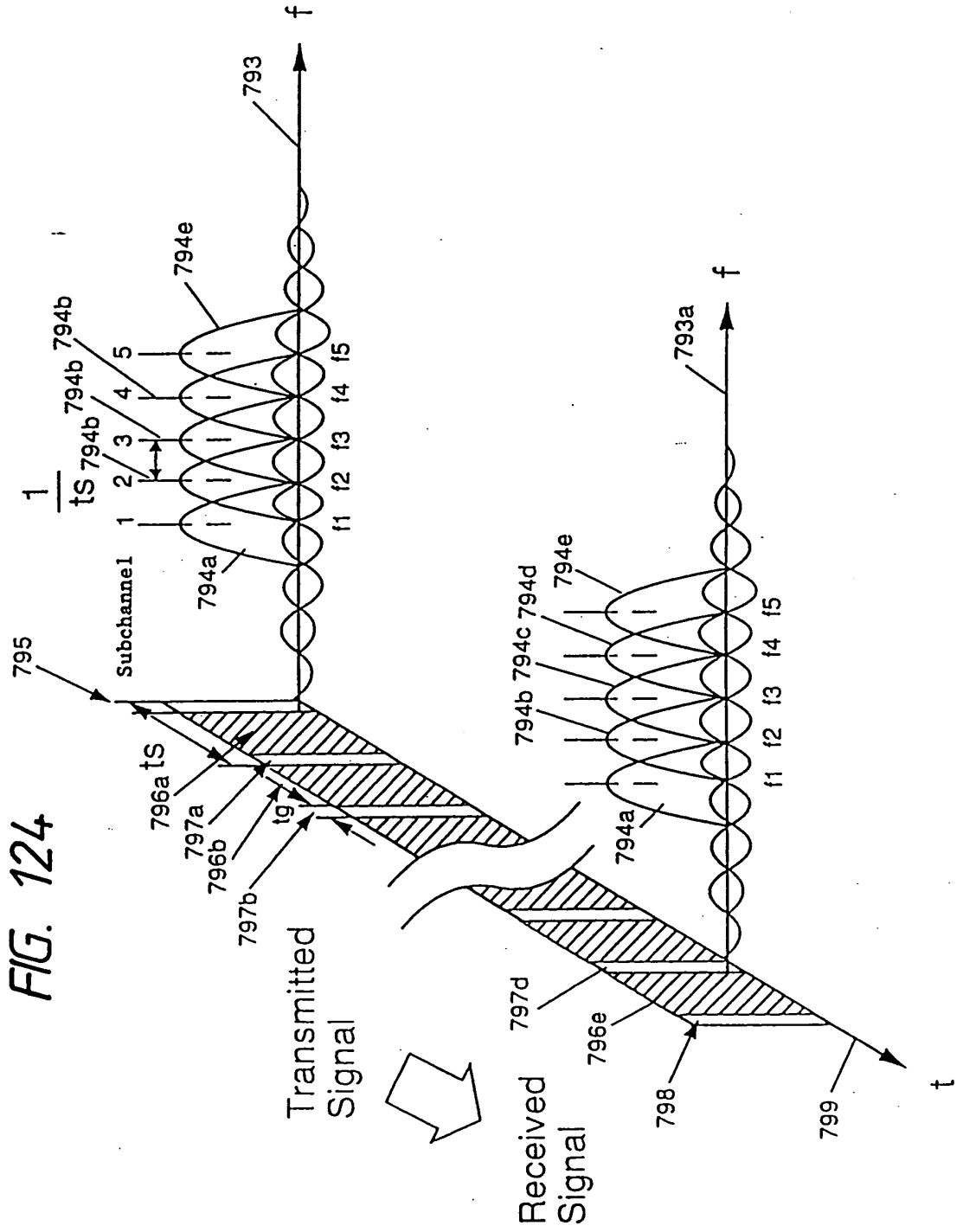
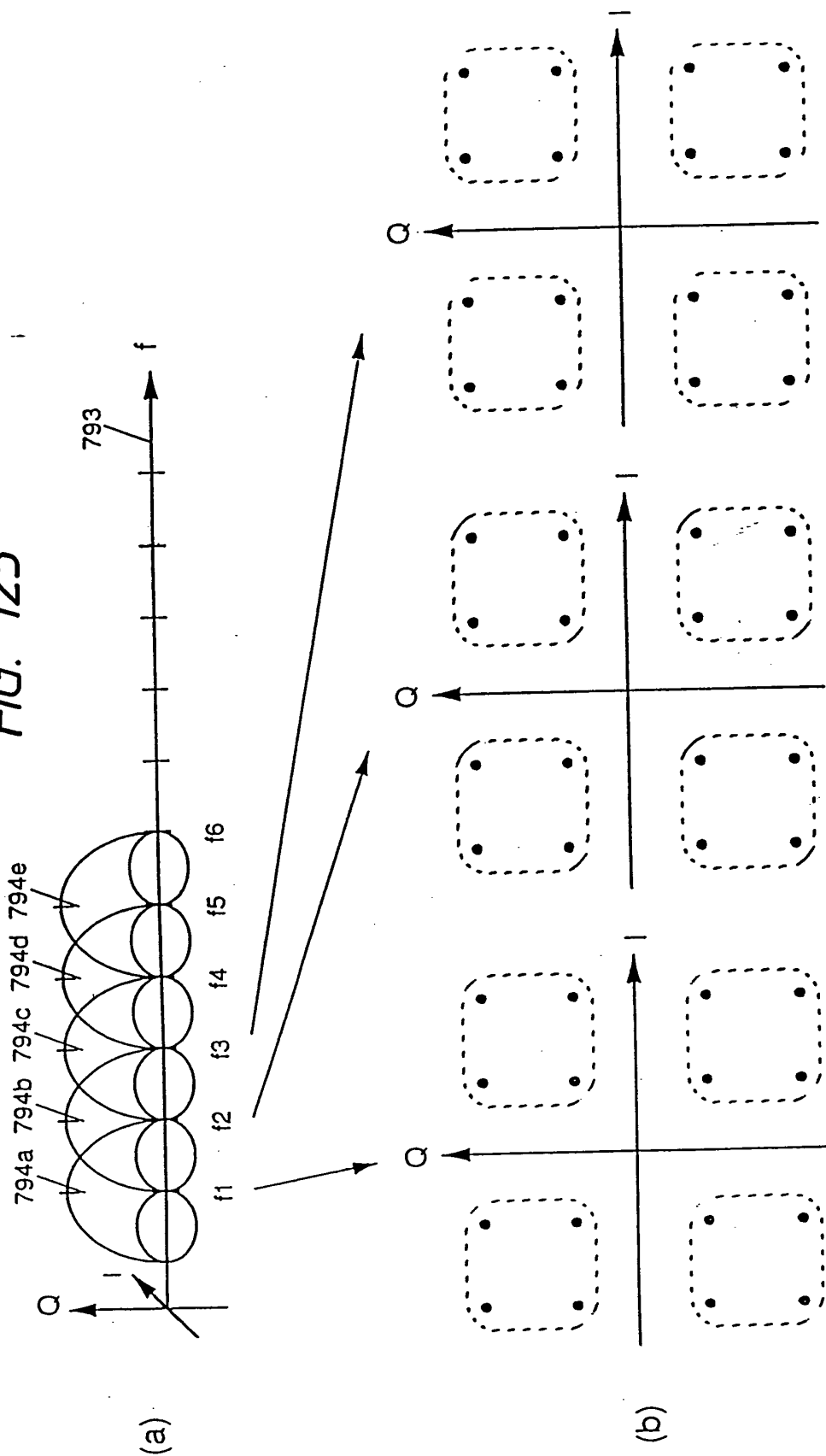


FIG. 125



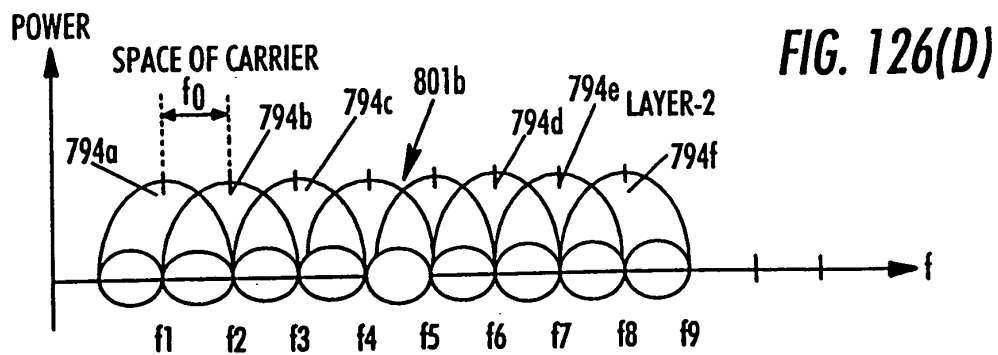
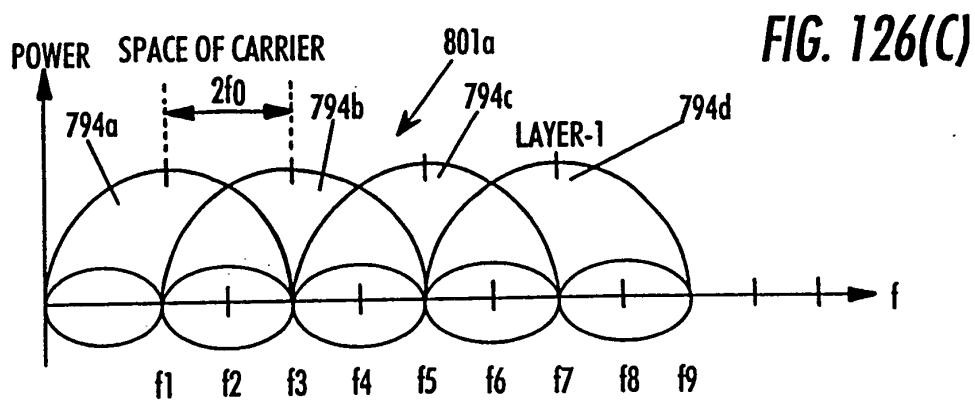
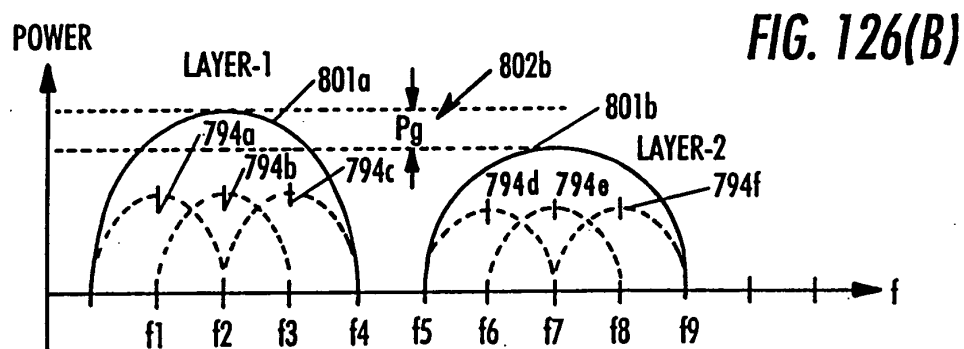
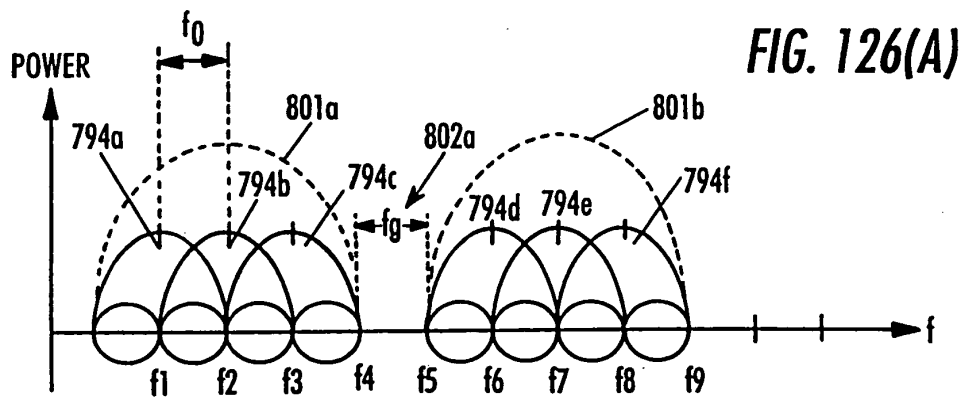


FIG. 127

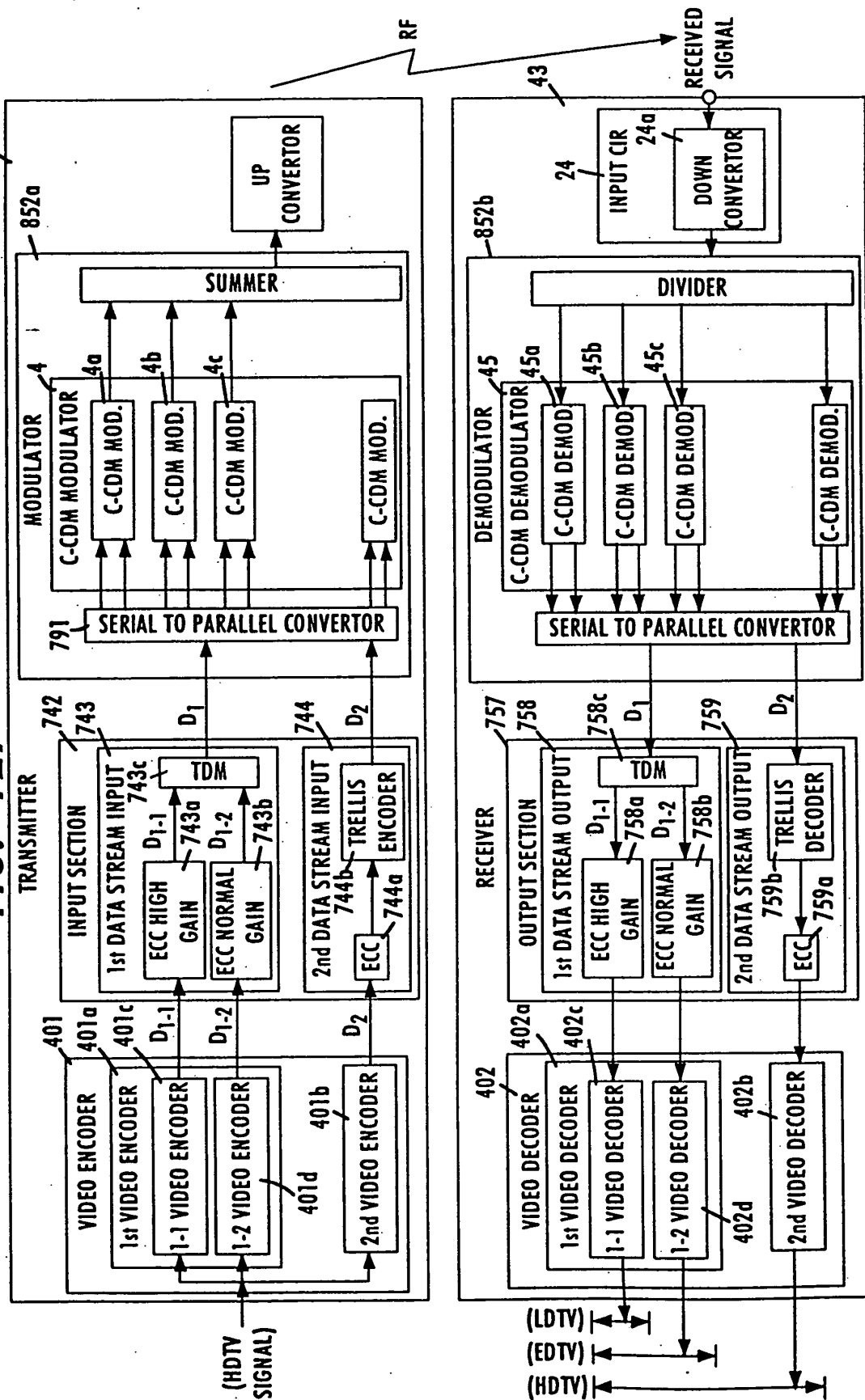


FIG. 128

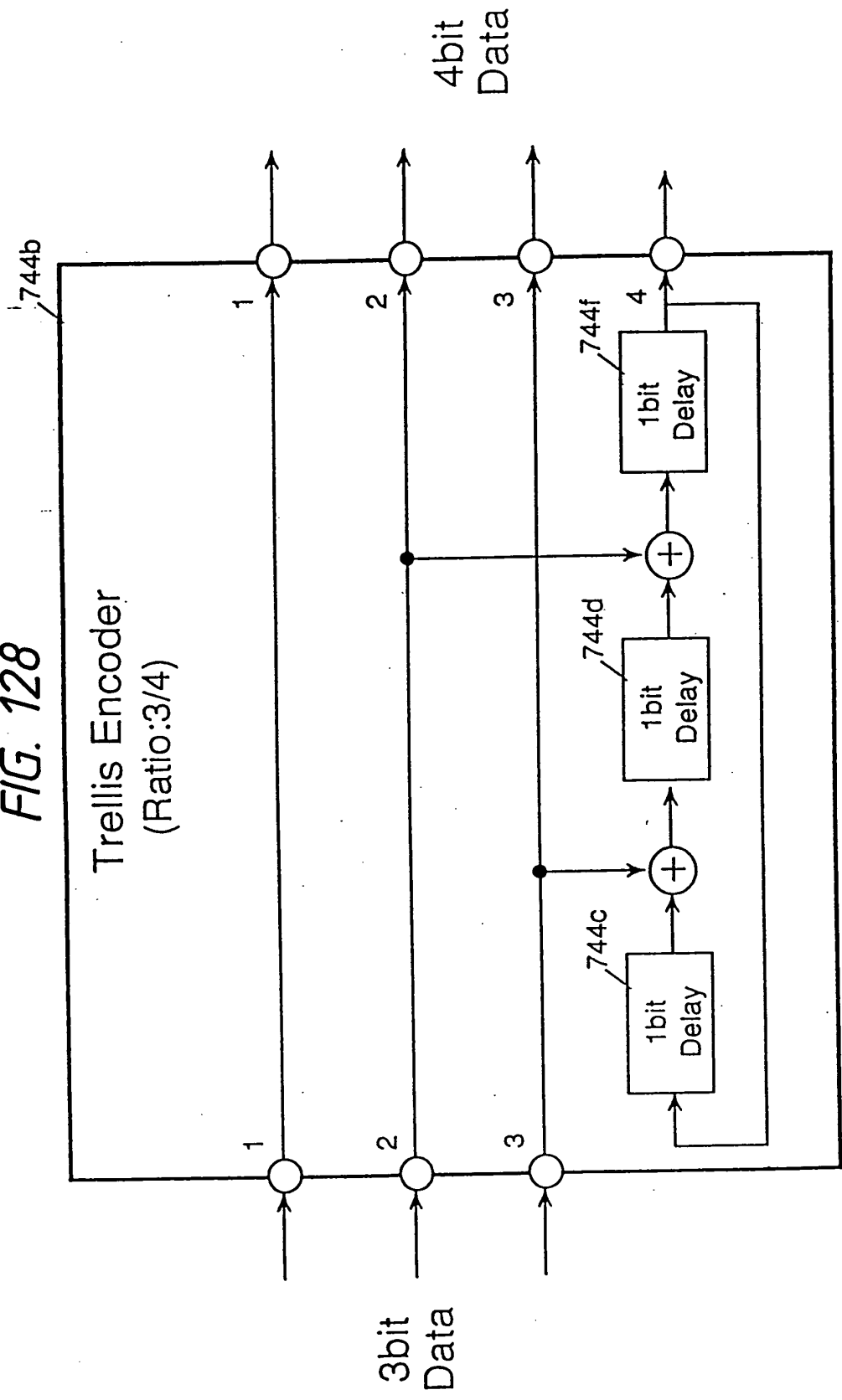


FIG. 129

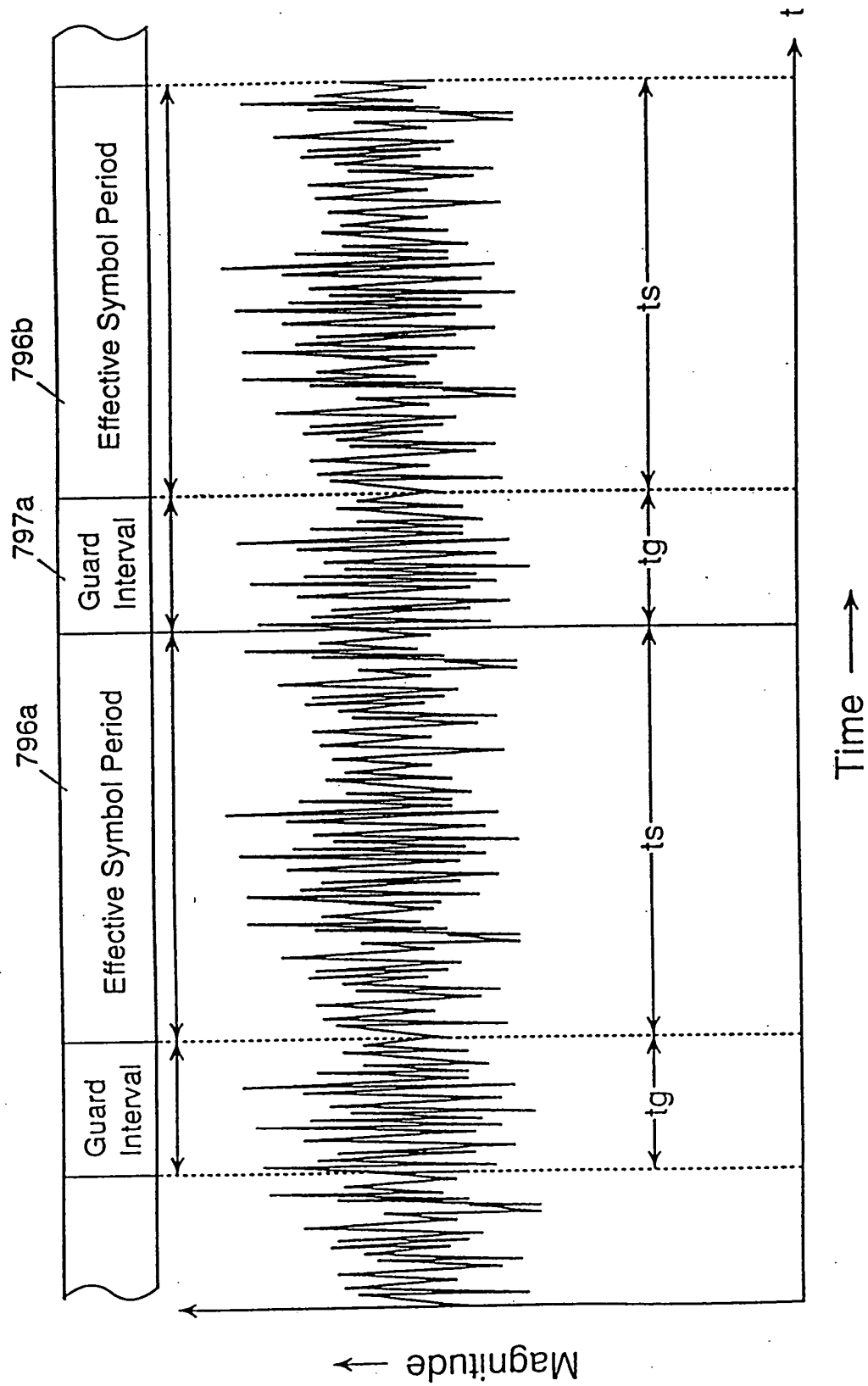


FIG. 130

GHOST DELAY = 2 μ s. D/U = 8dB
 FIGURE 8 BIT ERROR RATE PERFORMANCE UNDER SINGLE GHOST
 AND GAUSSIAN NOISE (1)

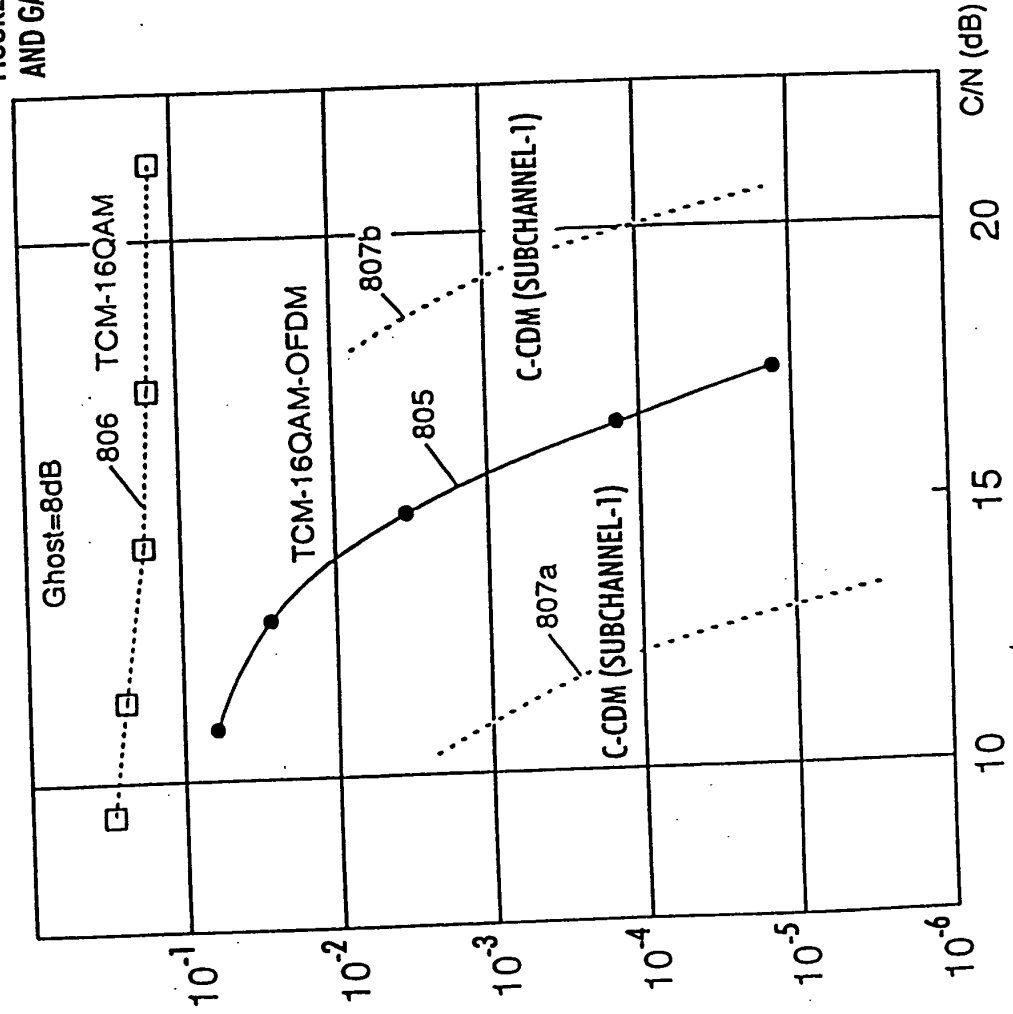


FIG. 131

MAGNETIC RECORDING/PLAYBACK APPARATUS

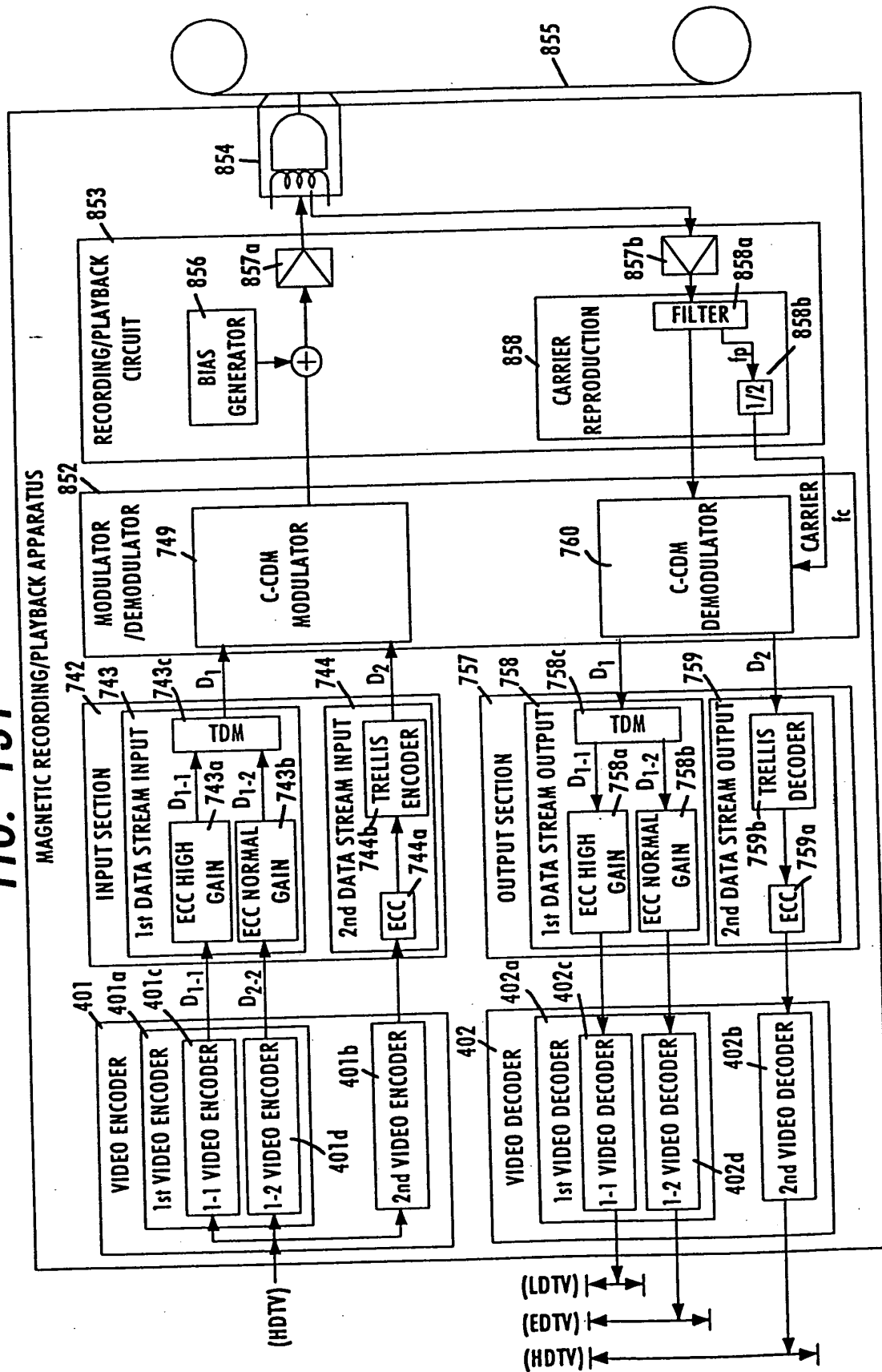


FIG. 133

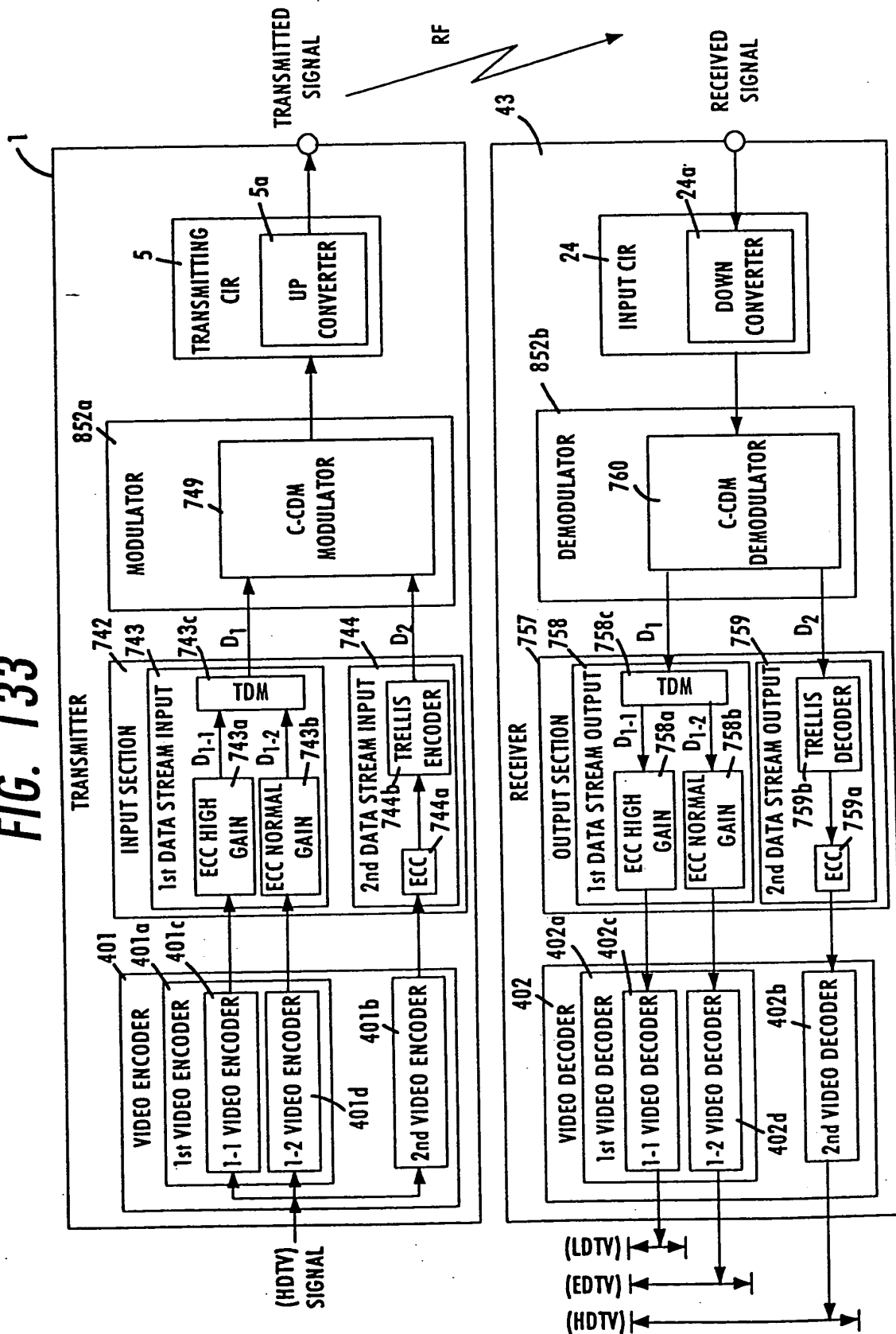


FIG. 134

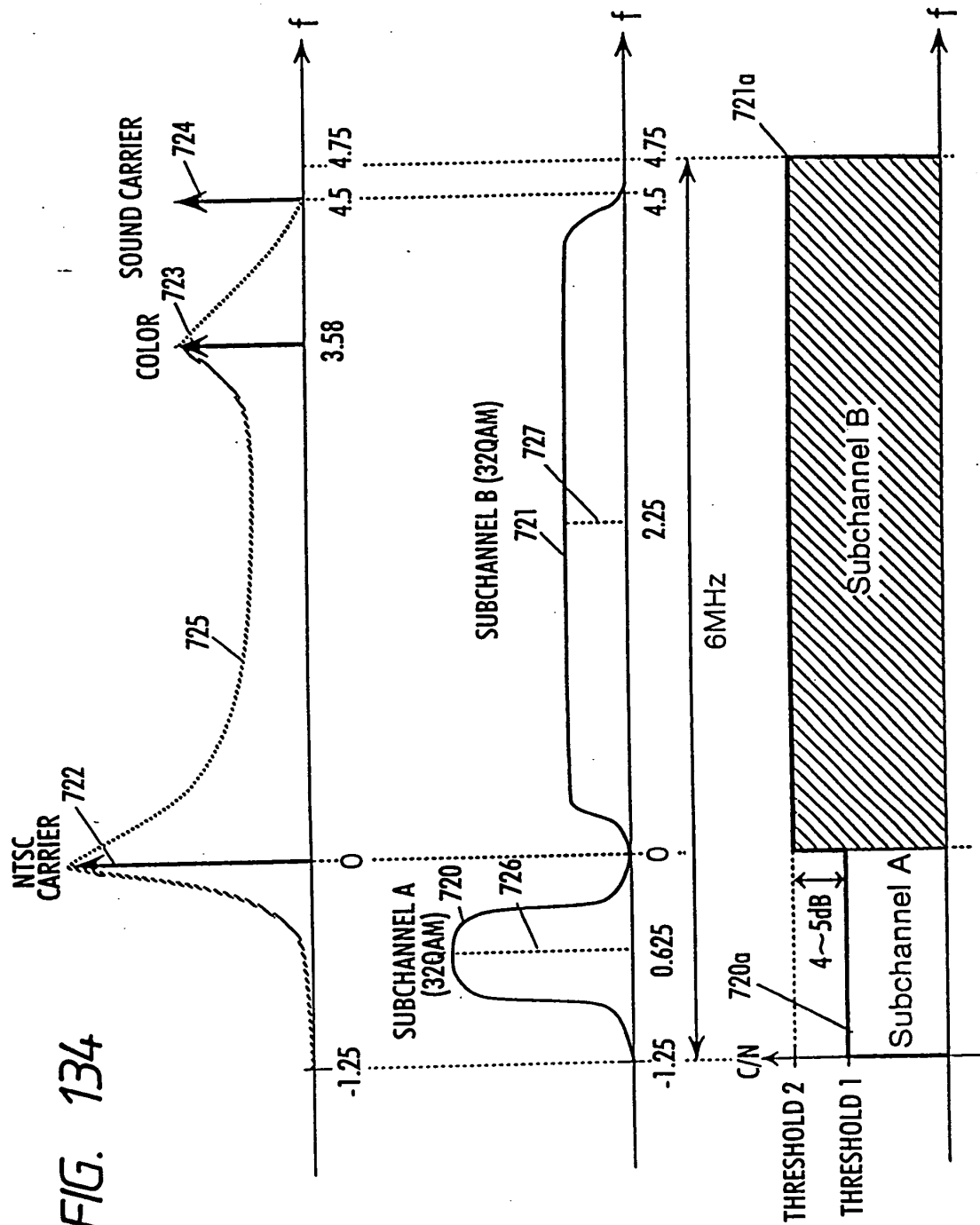


FIG. 135

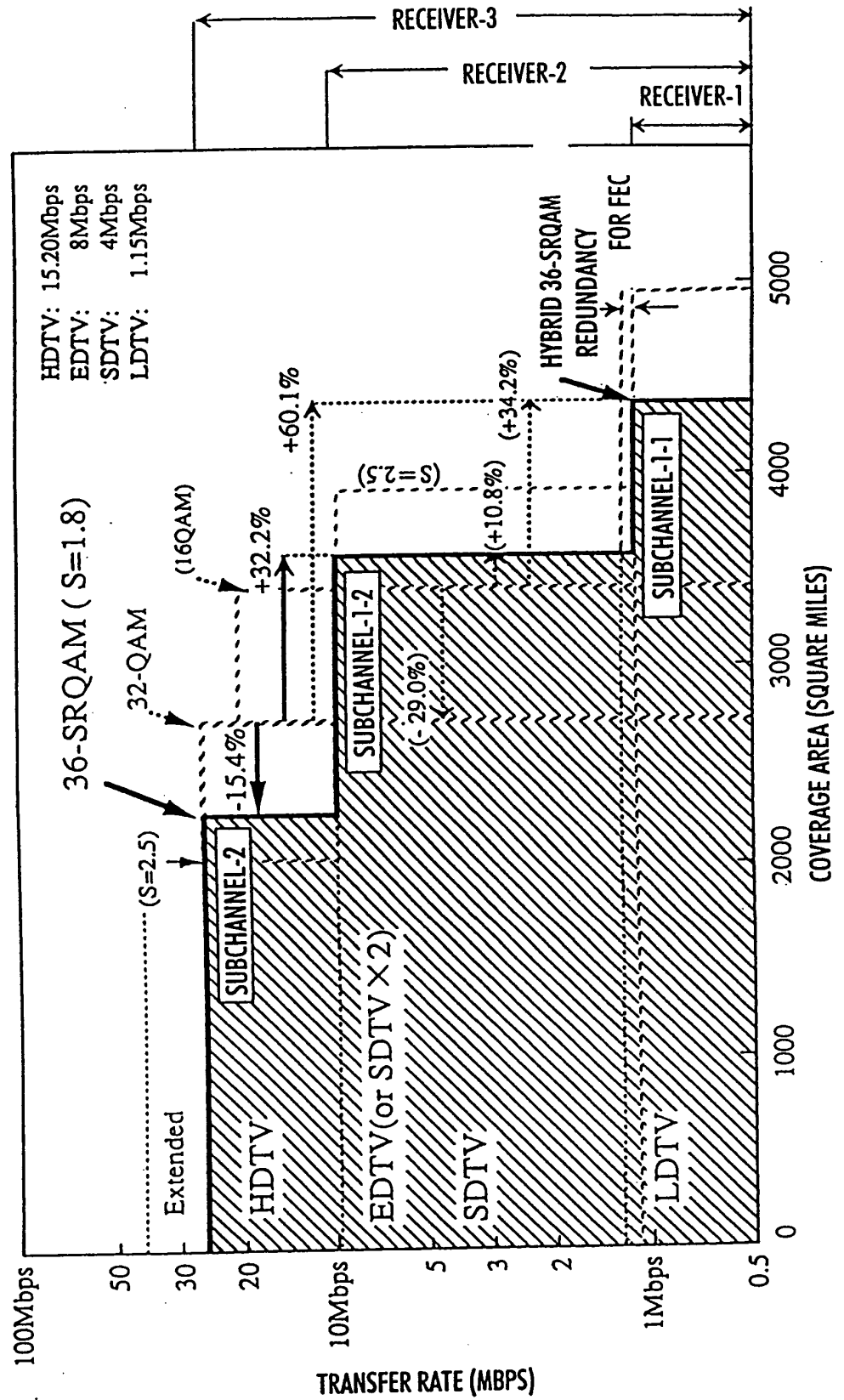


FIG. 136

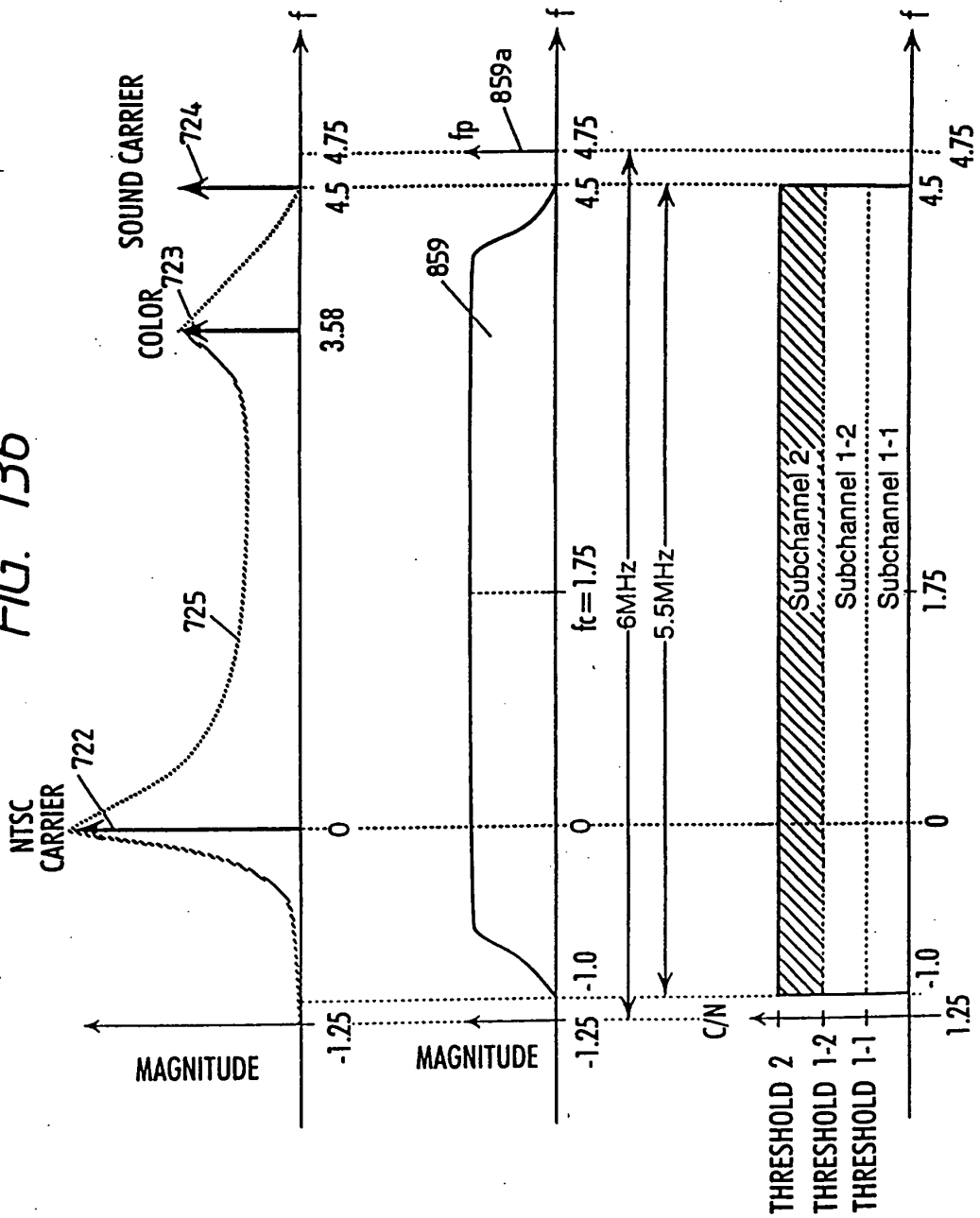


FIG. 137

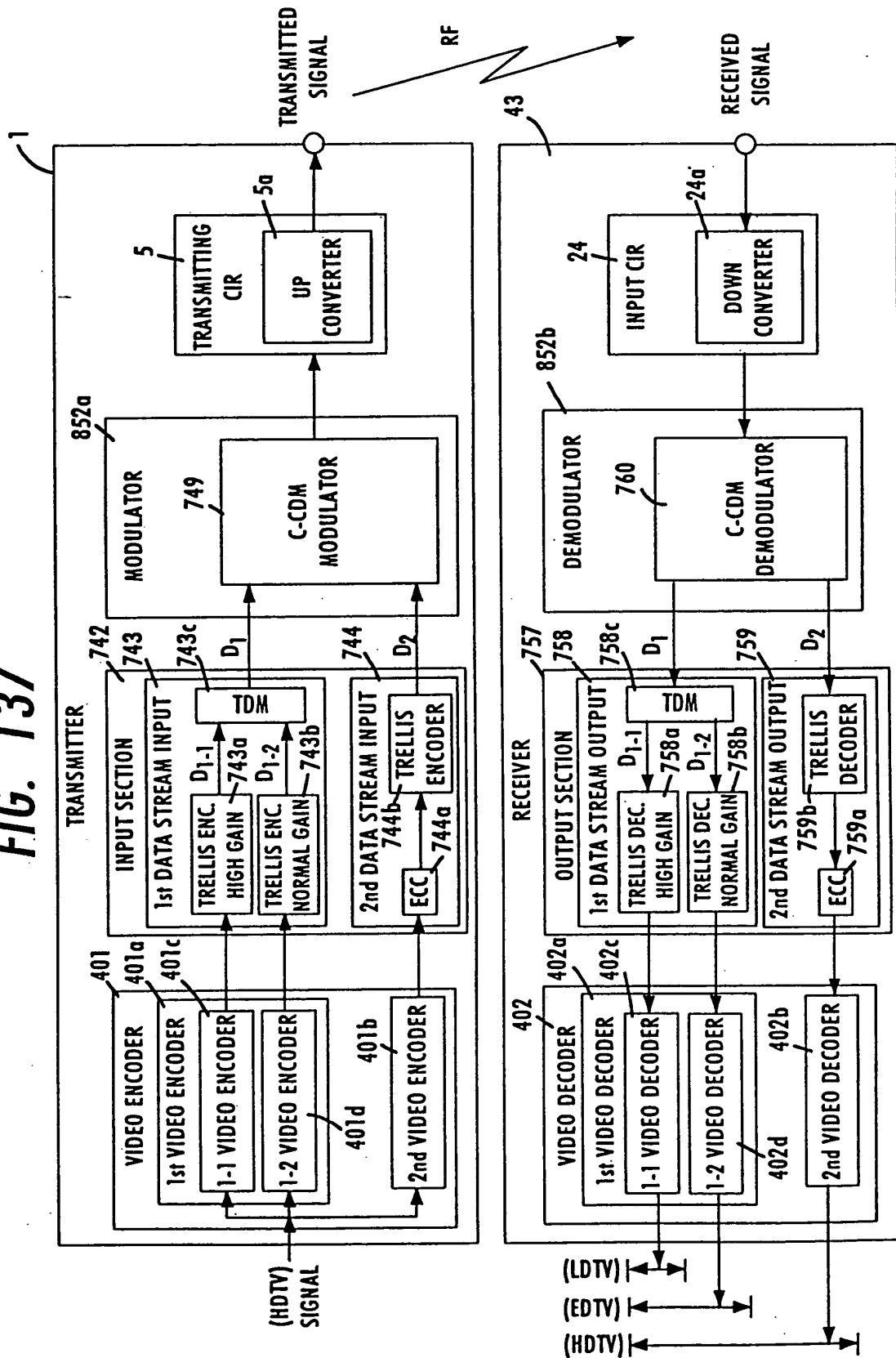


FIG. 138

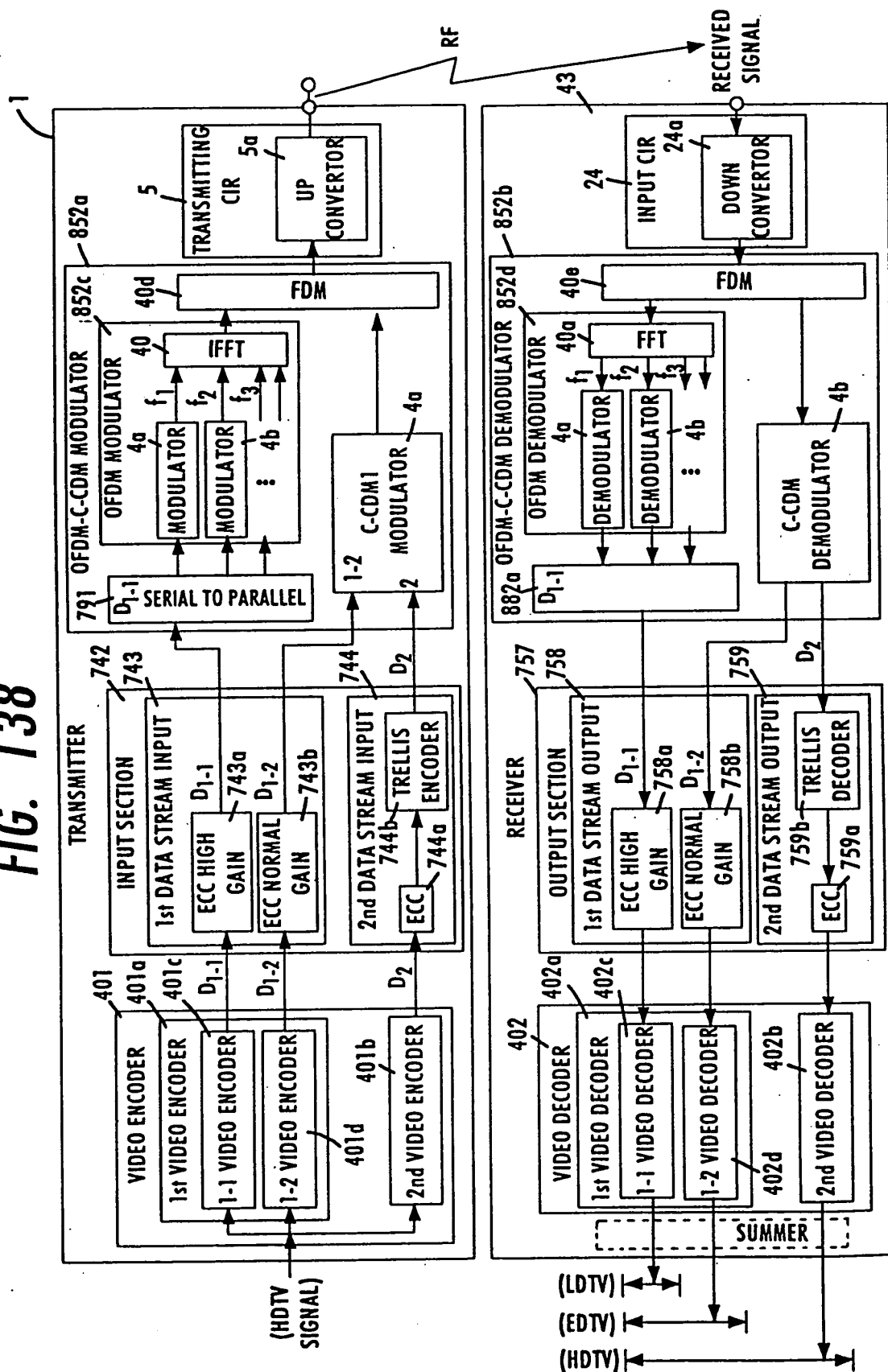


FIG. 139

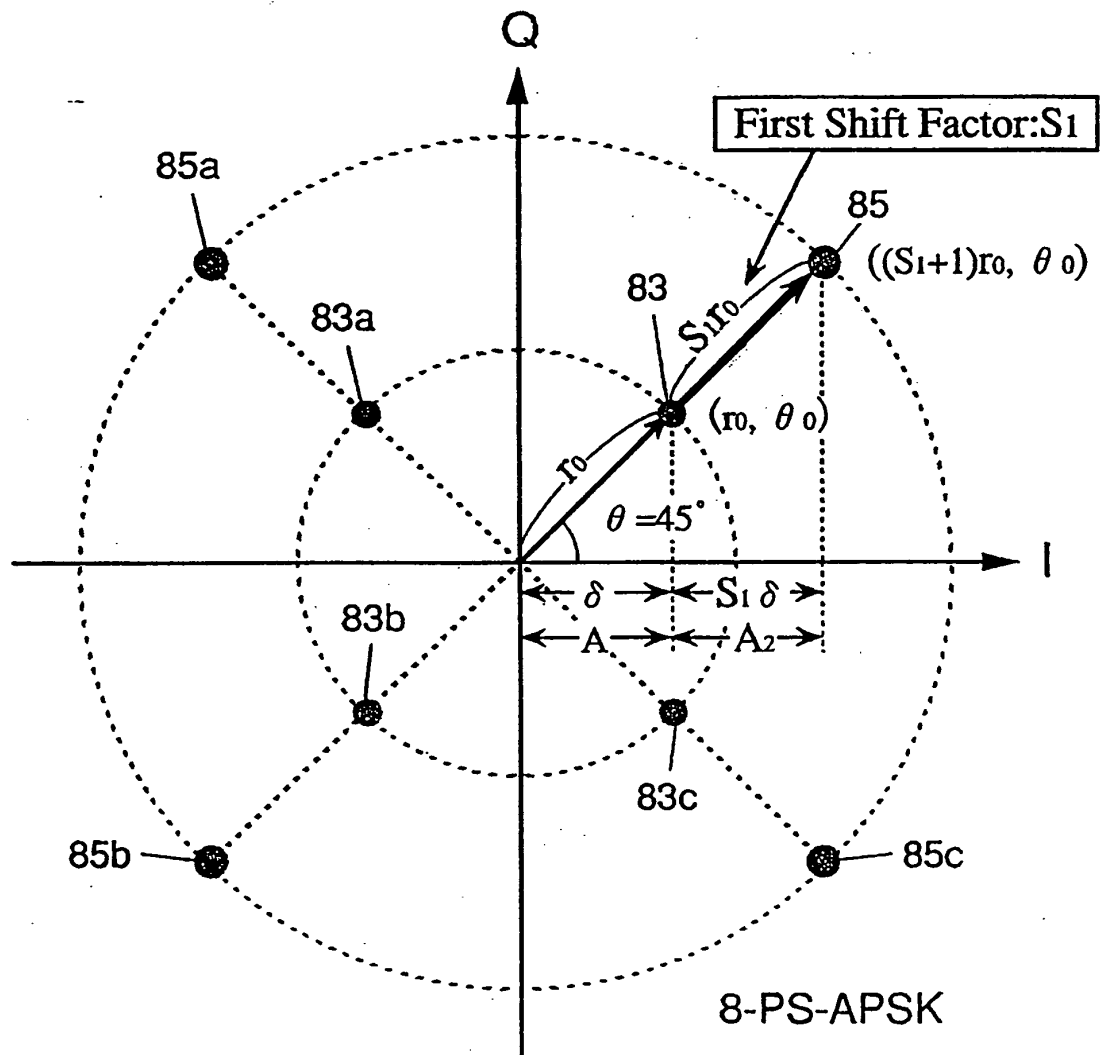


FIG. 140

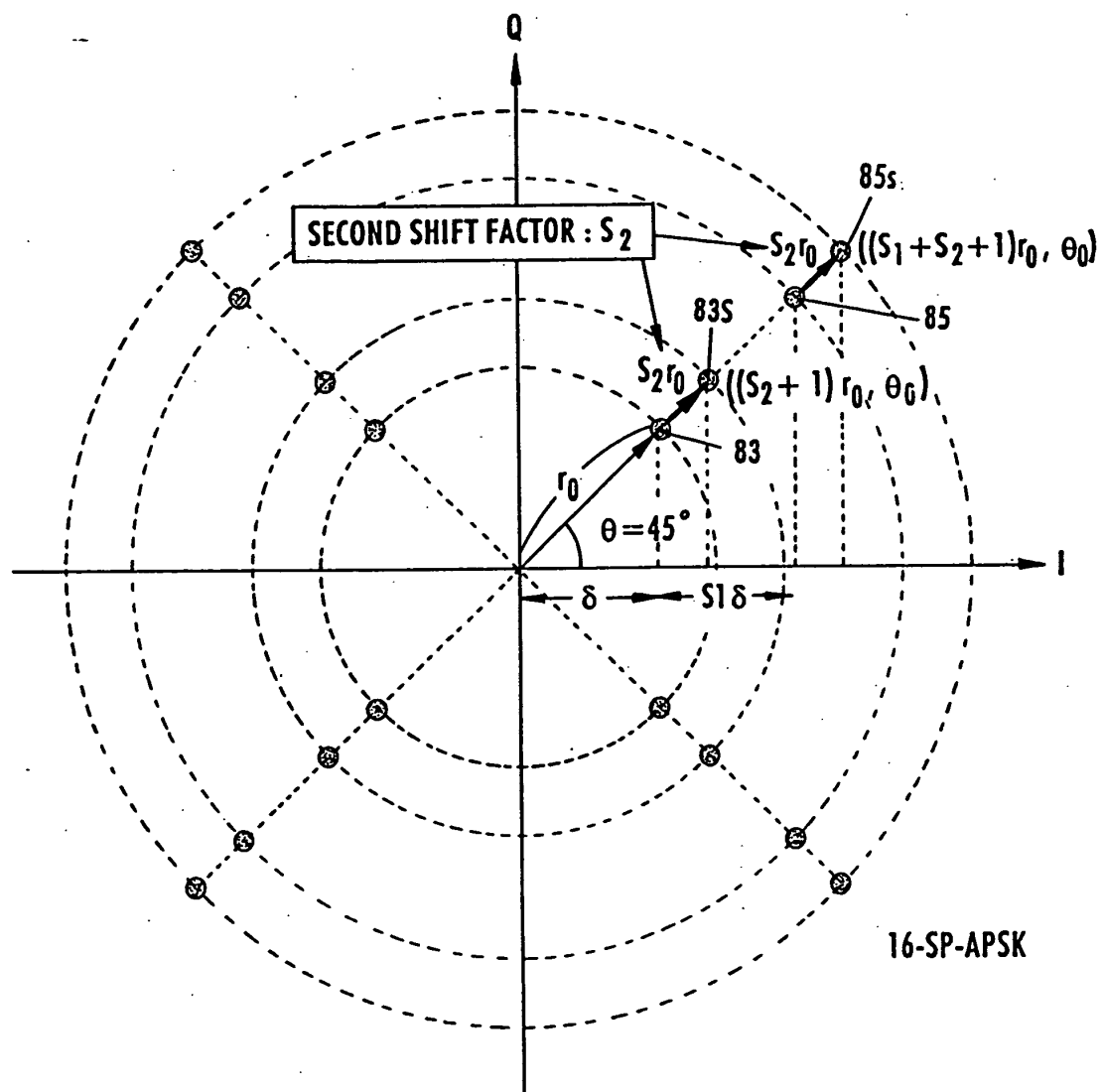


FIG. 141

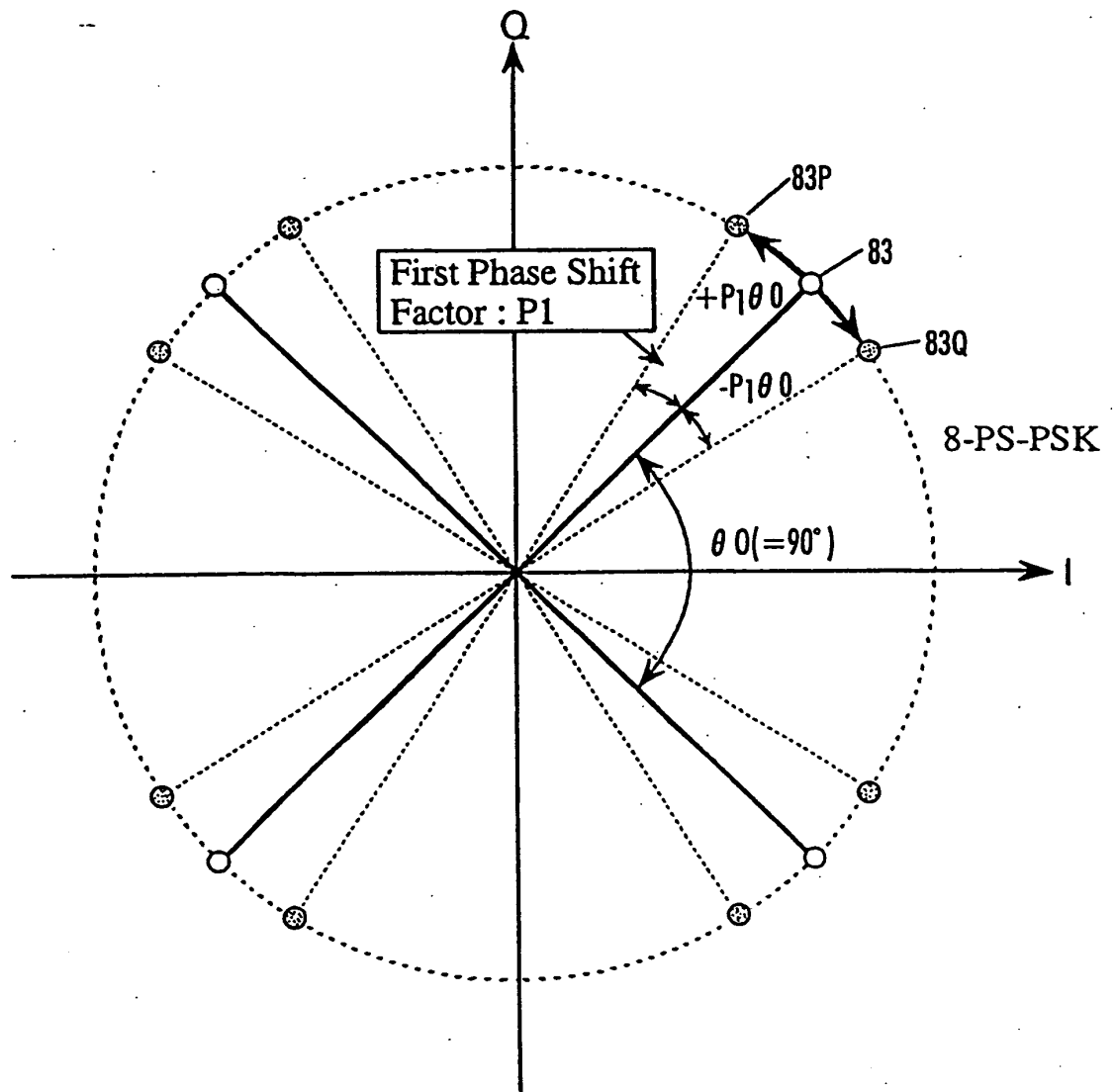


FIG. 142

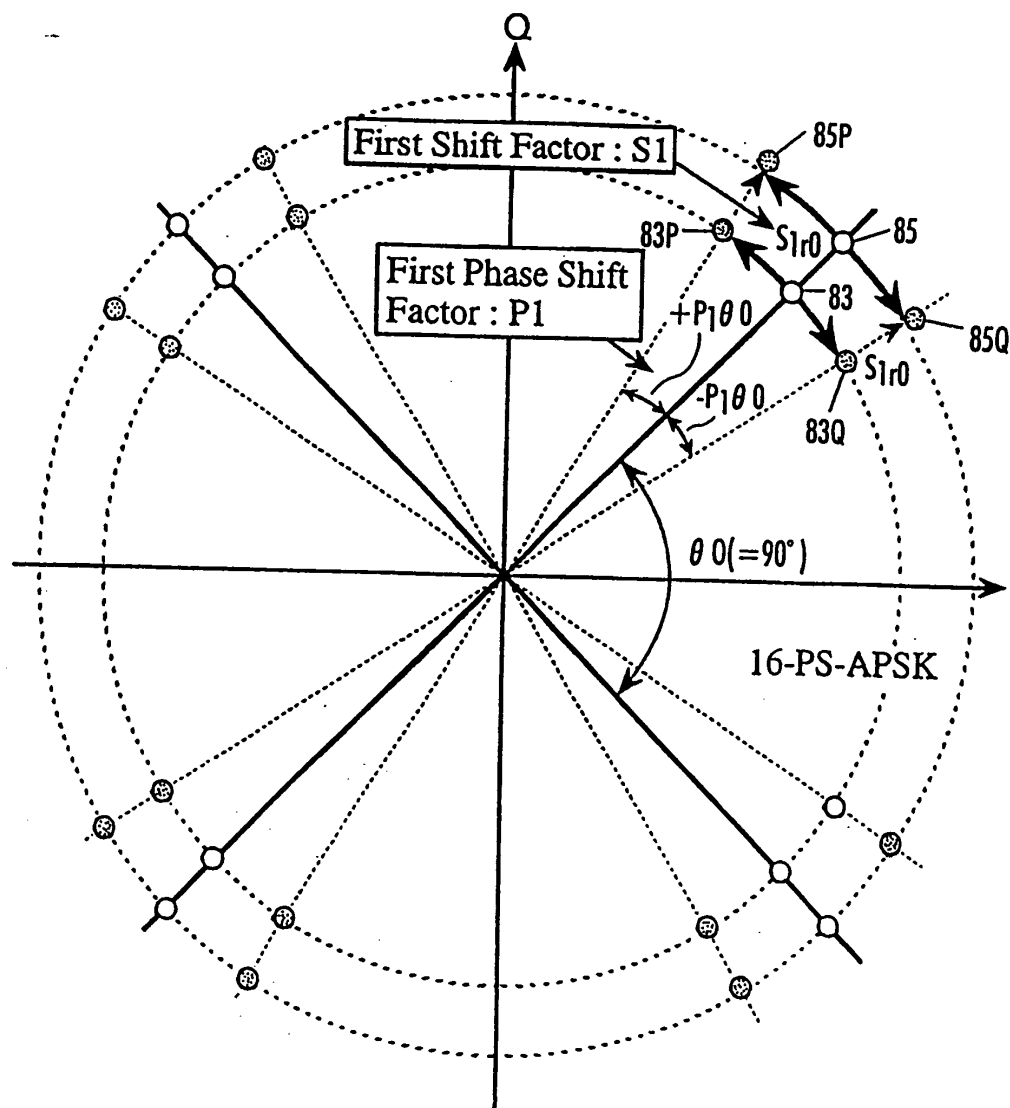


FIG. 143

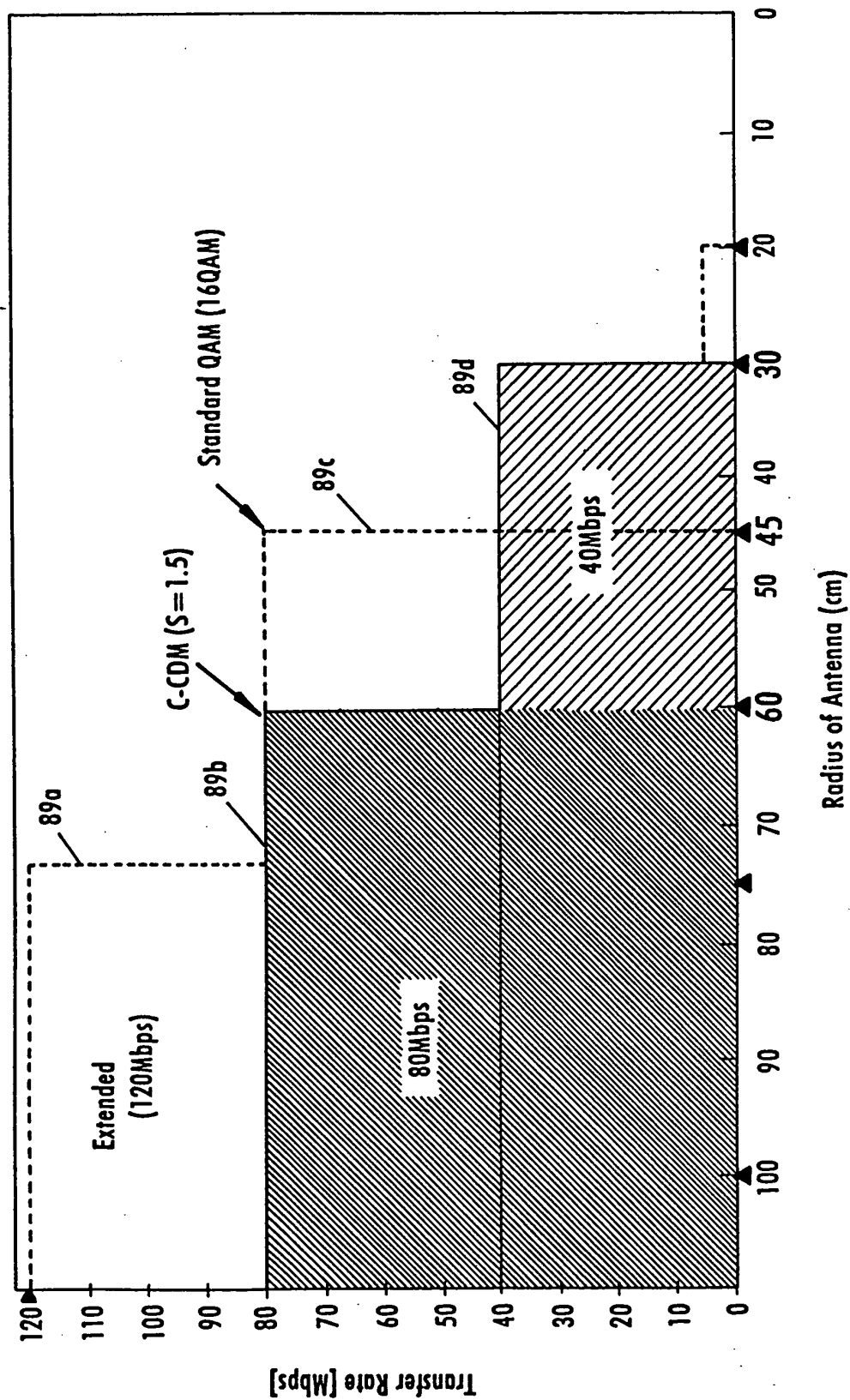


FIG. 144

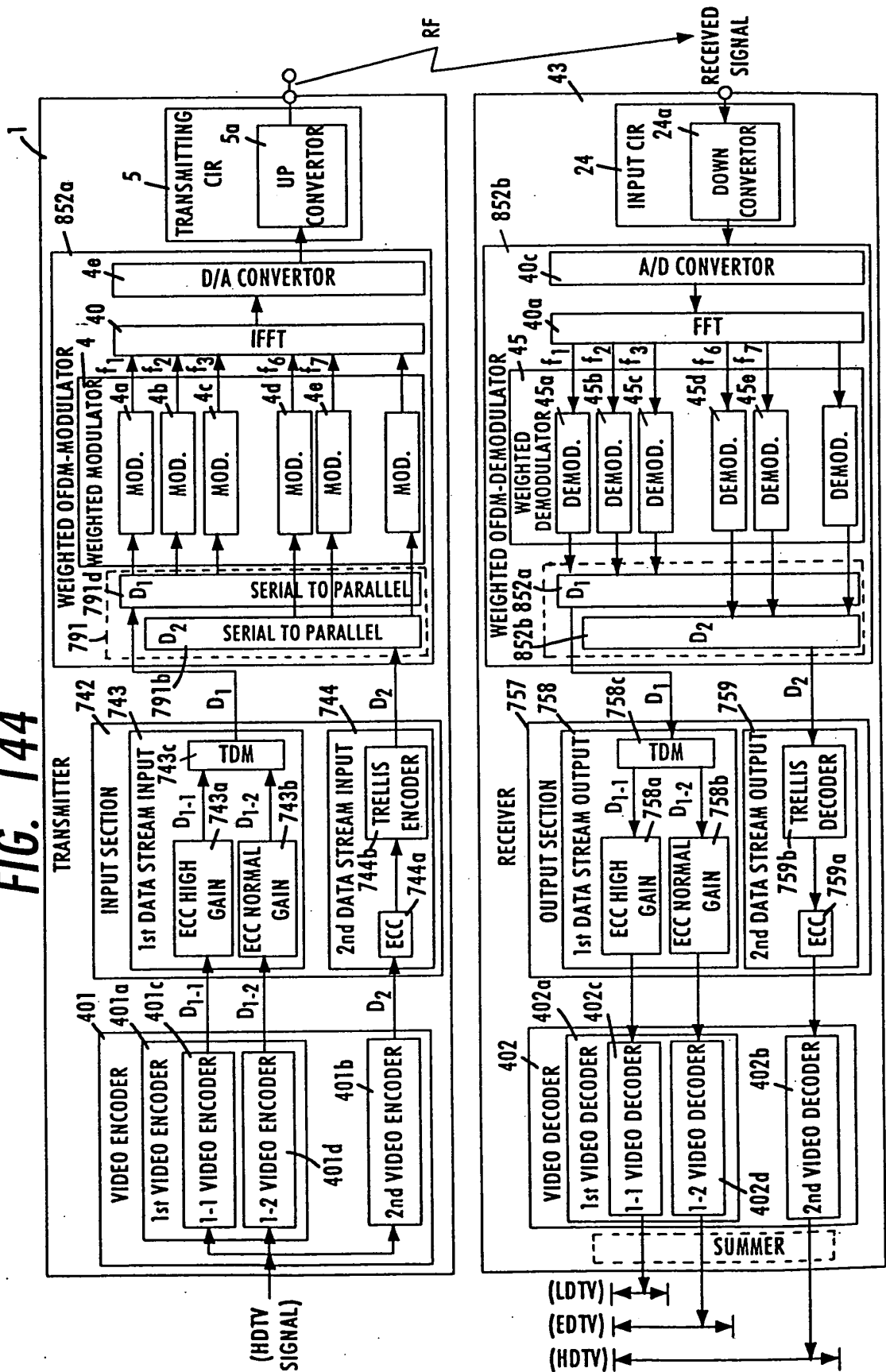


FIG. 145(A)

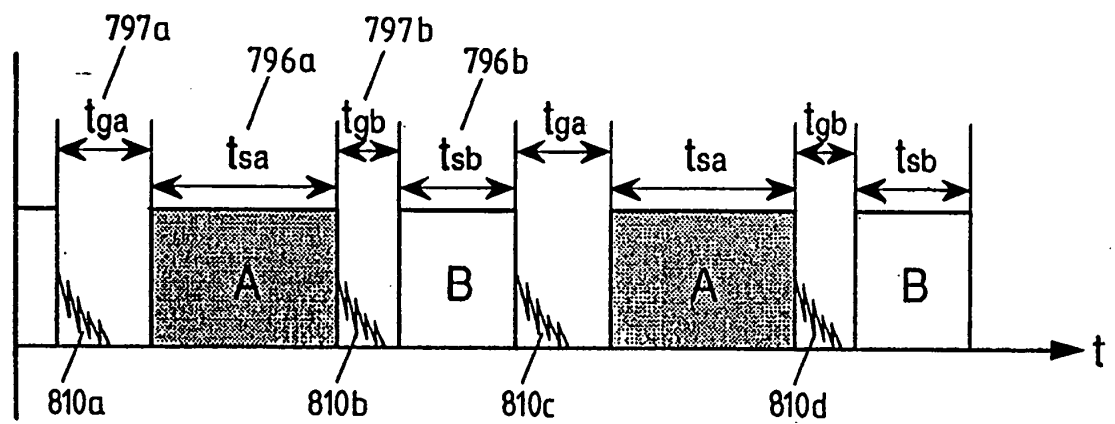


FIG. 145(B)

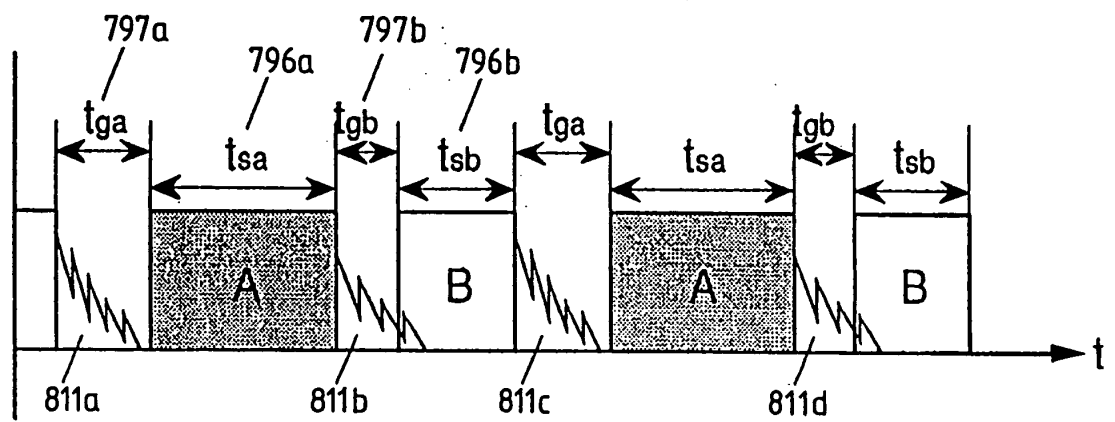
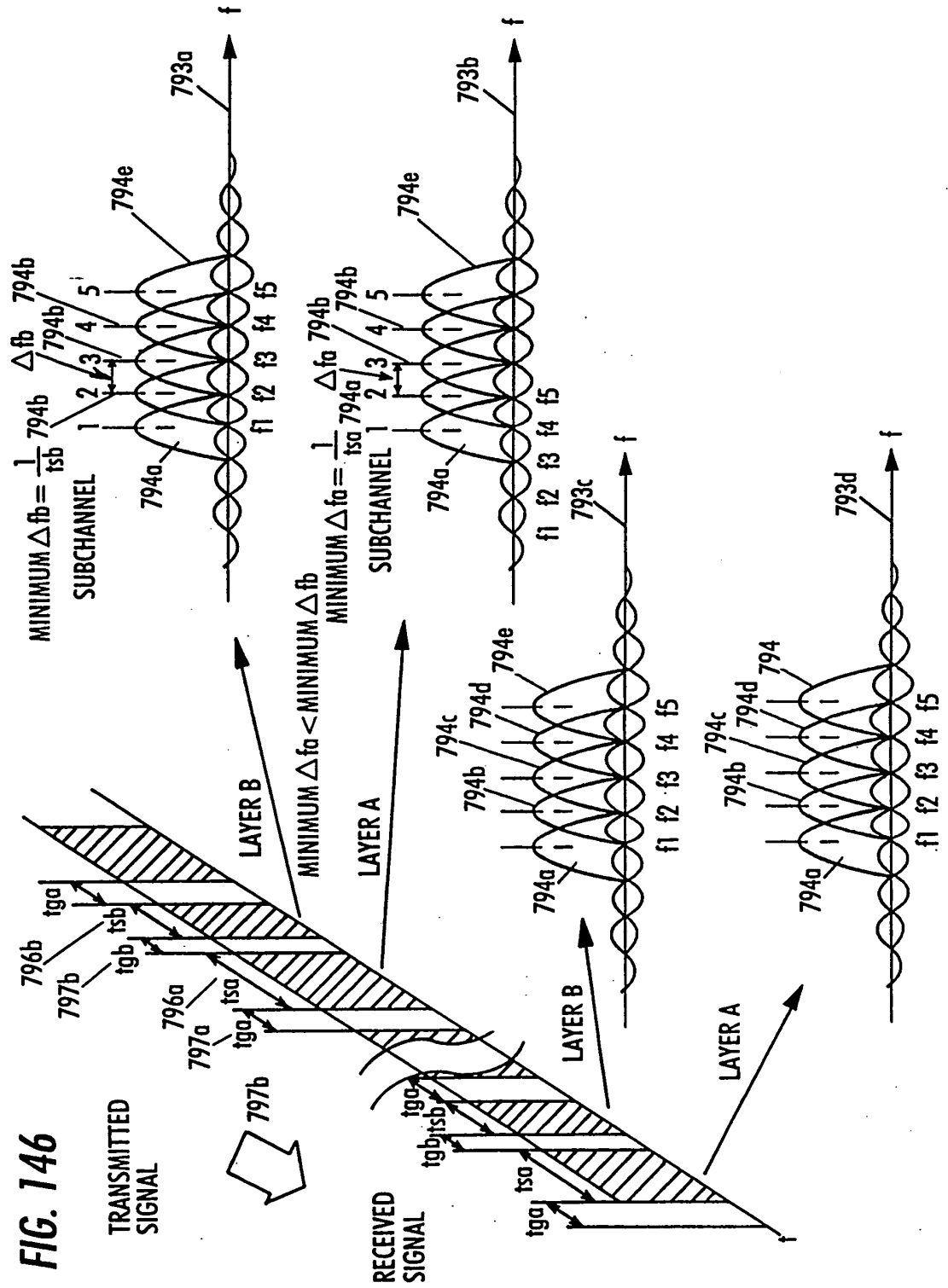


FIG. 146



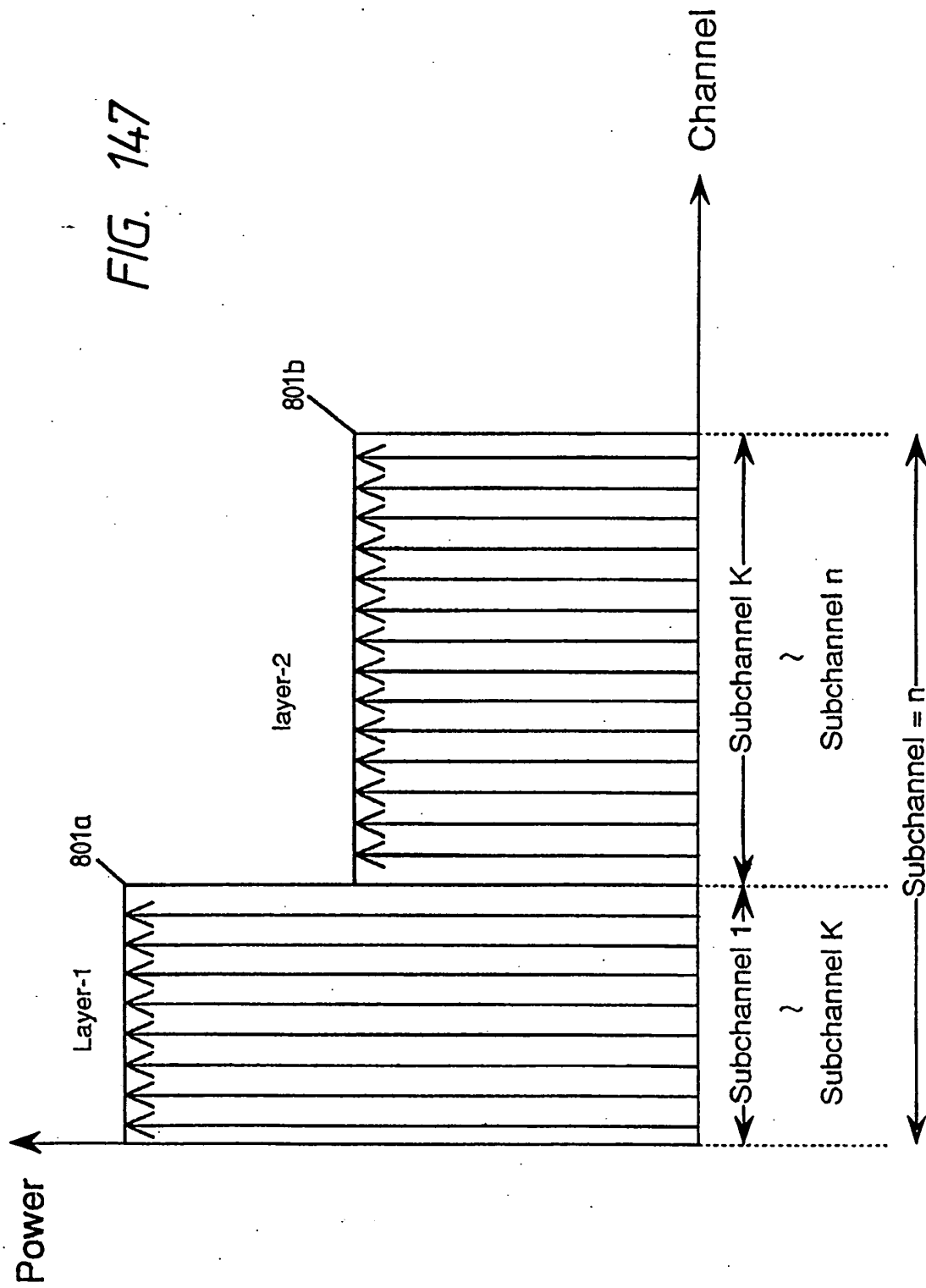
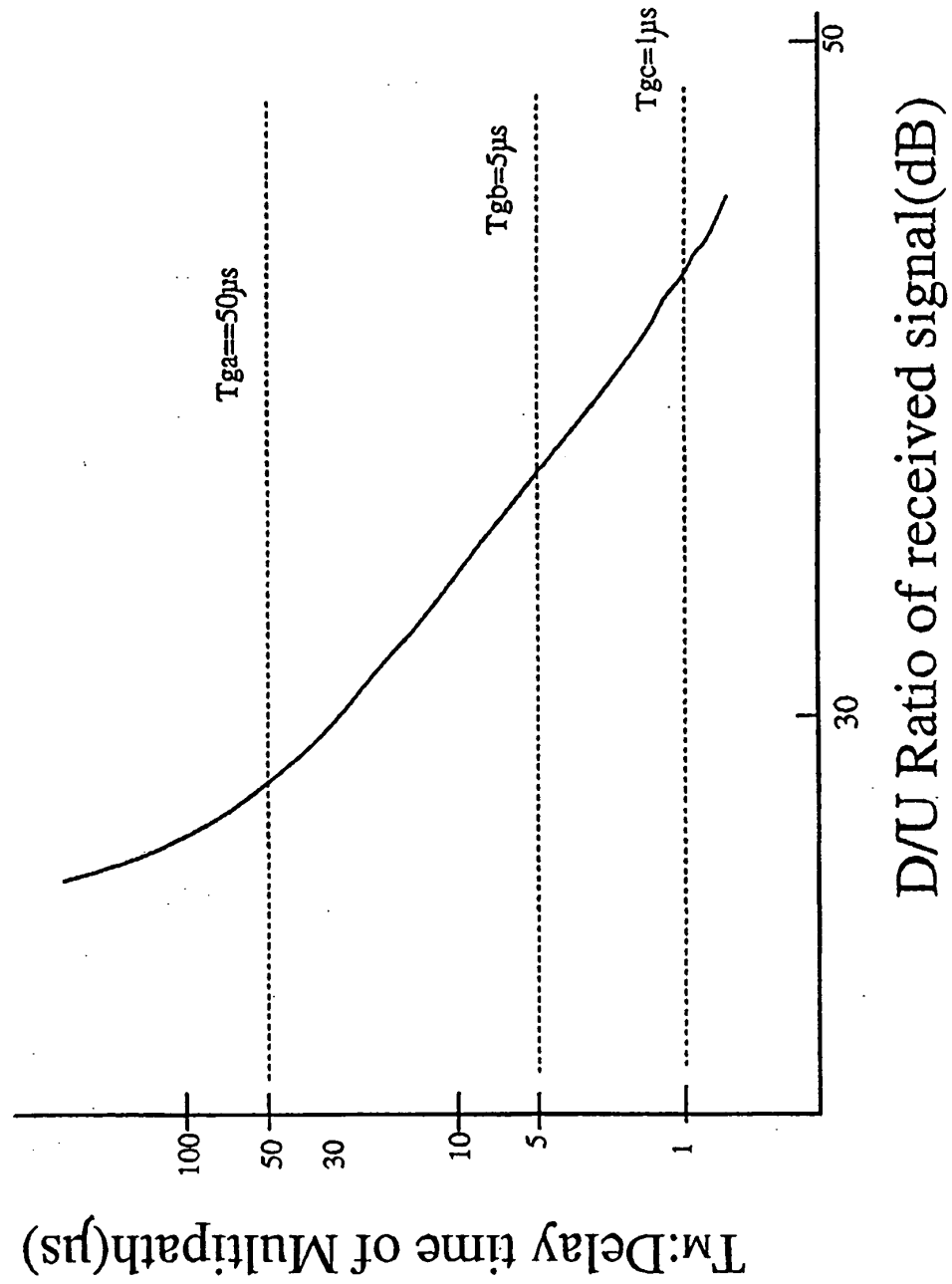


FIG. 147

FIG. 148



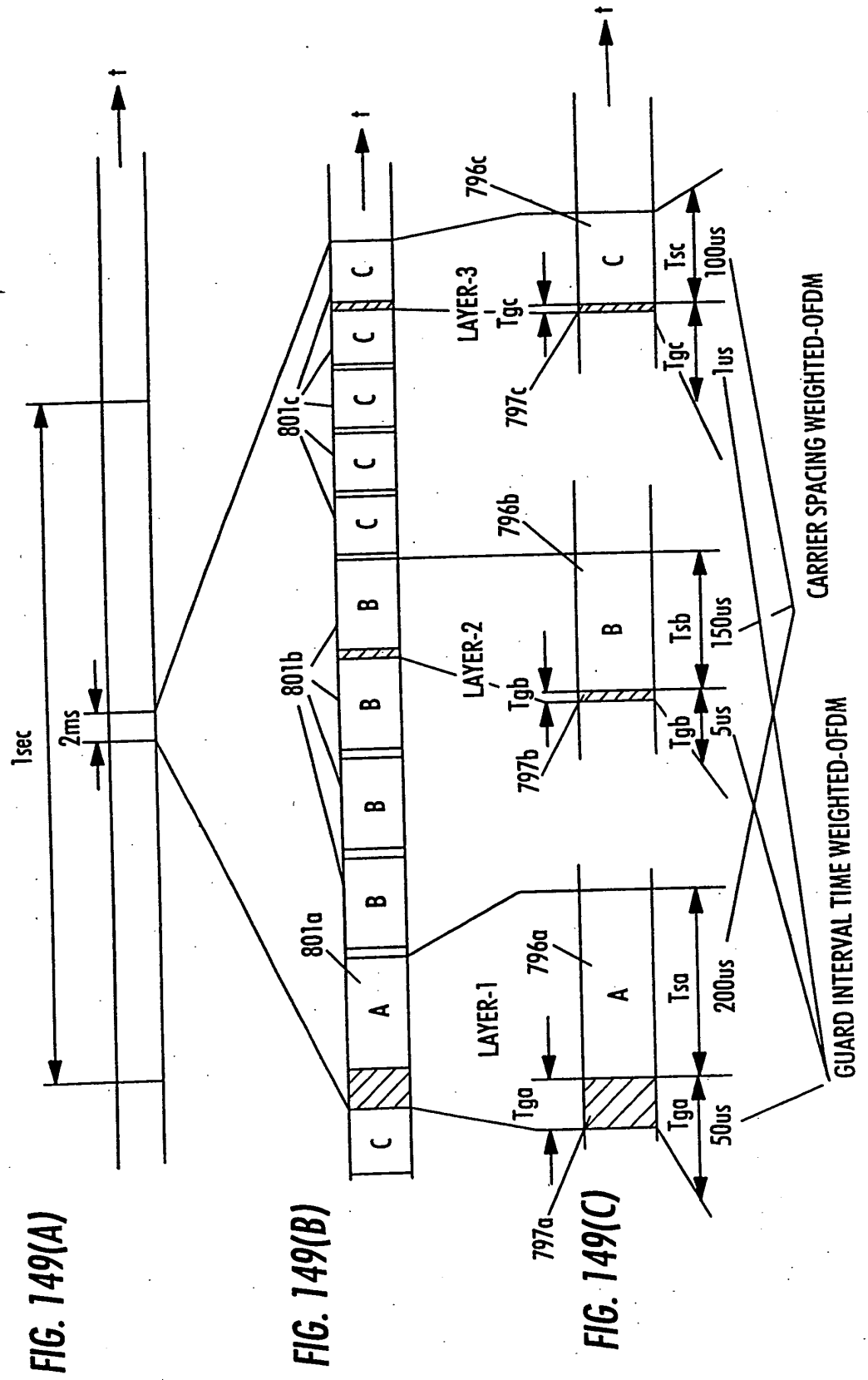


FIG. 150

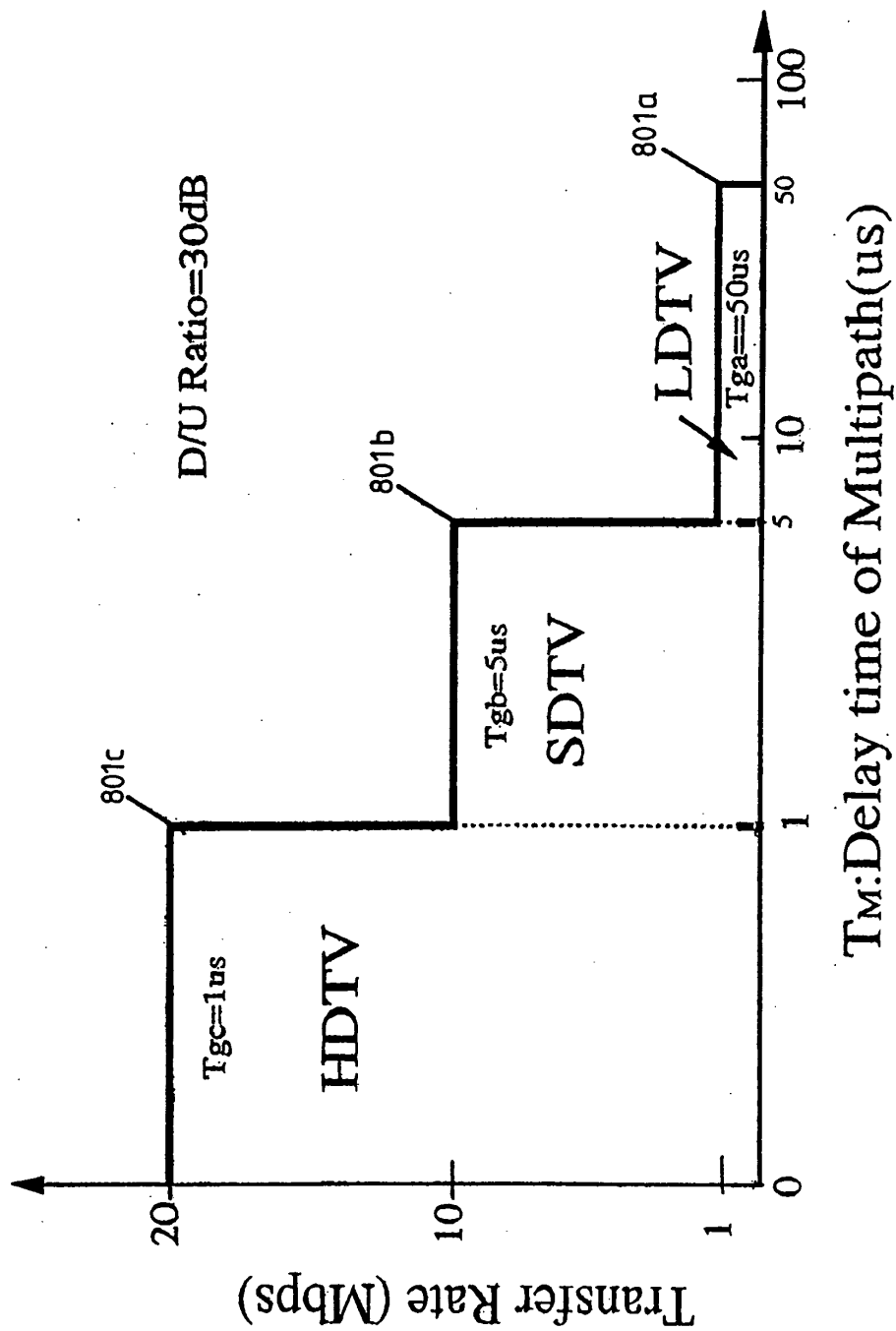


FIG. 151

